GENERAL NOTES

A. ▭ INDICATES FRONT PANEL MARKINGS.

B. IF NECESSARY, REFER TO FIGURE 5-13, FOR TROUBLESHOOTING AND PARAGRAPH 3-4, FOR FUNCTIONAL DESCRIPTION.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

- CIRCUIT GROUND
- PULLUP
- TO
- FROM
- TEST POINT
- CHASSIS GROUND

SPECIFIC NOTES

1. THE ADDRESS BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR J1, J2, J3, AND J4. THE FOLLOWING IS THE ROUTING LIST:

ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE
AB00	J2-A28	AB06	J2-B29	AB11	J2-B28
AB01	J2-A27	AB07	J2-B30	AB12	J2-A32
AB02	J2-A29	AB08	J2-B31	AB13	J2-A26
AB03	J2-B26	AB09	J2-B32	AB14	J2-A25
AB04	J2-A30	AB10	J2-B27	AB15	J2-B25
AB05	J2-A31				

2. FOR IDENTIFICATION OF PART NUMBER AND MESSAGE NUMBER ONLY SWITCHES S13 AND S14 ARE SHOWN. THE FOLLOWING TABLE IDENTIFIES THE REMAINING NUMBER SWITCHES.

KEY NO. (TOP/LOWER)	SWITCH NO.	"Y" INPUT	"X" OUTPUT	P1 PIN
!/1	S6	Y0C	X6C	11
"/2	S5	Y0C	X5C	2
#/3	S4	Y0C	X4C	1
$/4	S3	Y0C	X3C	4
%/5	S2	Y0C	X2C	3
&/6	S1	Y0C	X1C	14
'/7	S11	Y1C	X1C	14
(/8	S12	Y1C	X2C	3

3. THE TRANSMITTED SIGNALS, TXD1, TXD2, AND TXD3 ARE BIPOLAR SIGNALS WITH A LOGIC HIGH OF APPROXIMATELY +5 VDC AND A LOGIC LOW OF APPROXIMATELY -5 VDC.

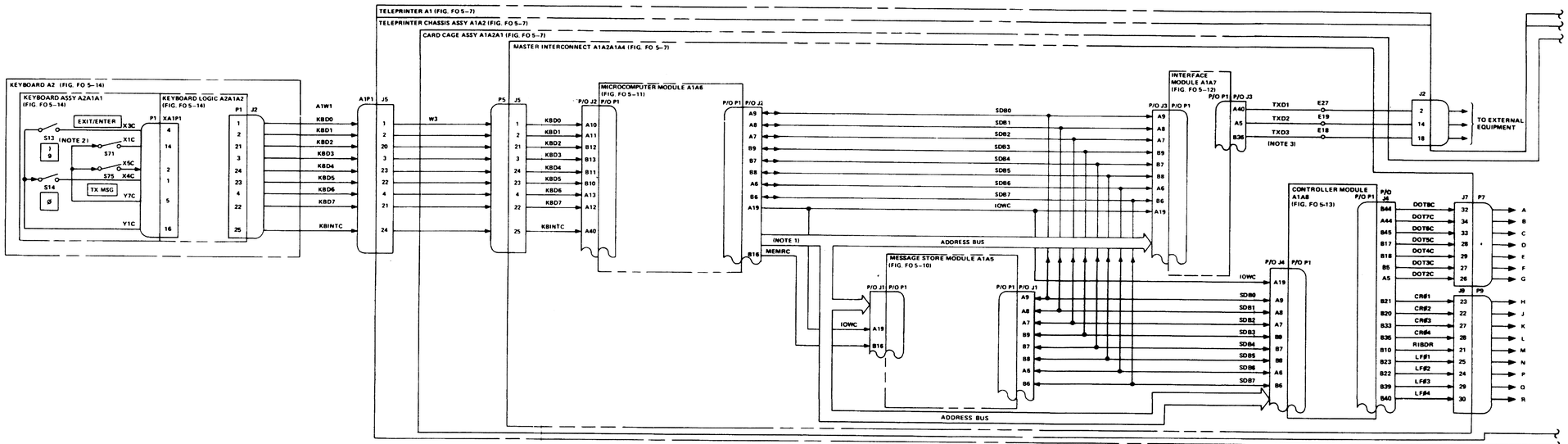


Figure FO 5-1. Transmit Function, Signal Flow Diagram (Sheet 1 of 2)

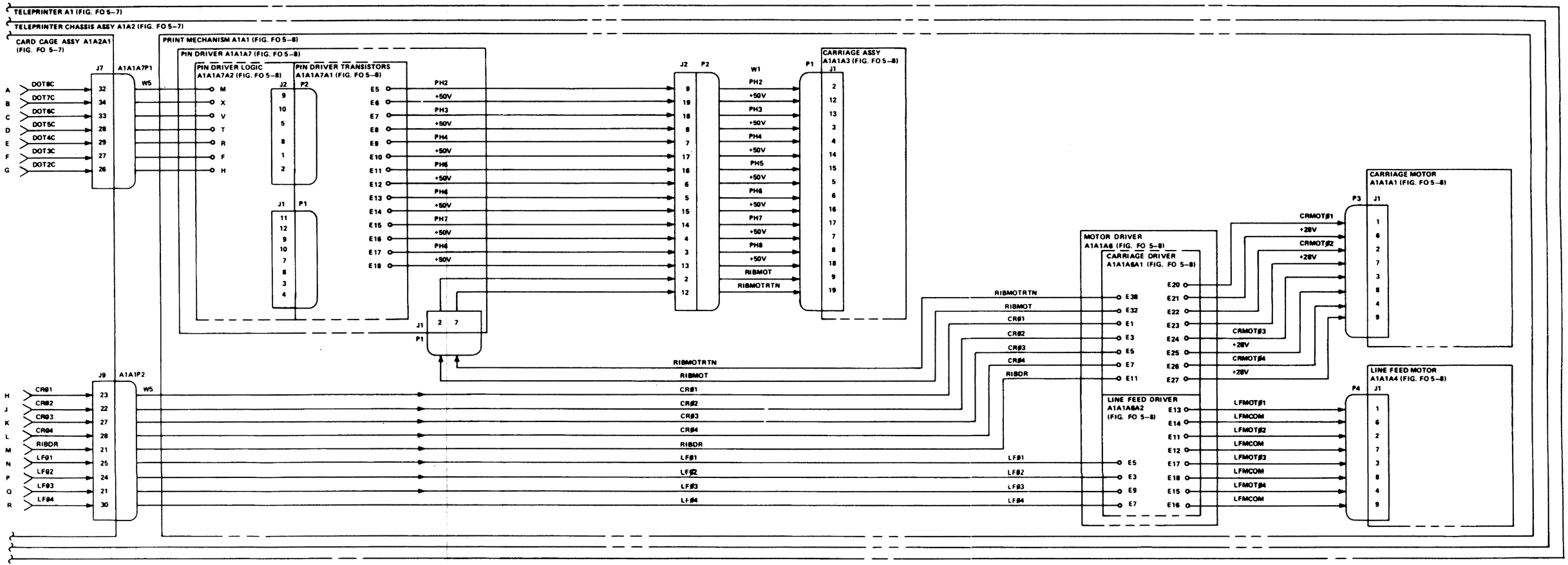


Figure FO 5-1. Transmit Function, Signal Flow Diagram (Sheet 2 of 2)

GENERAL NOTES

A. IF NECESSARY, REFER TO FIGURE 5-12, FOR TROUBLESHOOTING AND PARAGRAPH 3-5, FOR FUNCTIONAL DESCRIPTION.

B. [ ] INDICATES FRONT PANEL MARKINGS.

SPECIFIC NOTES

1. THE RECEIVED SIGNALS, RXD1, RXD2, AND RXD3, ARE BIPOLAR SIGNALS WITH A LOGIC HIGH OF APPROXIMATELY +5 VDC AND A LOGIC LOW OF APPROXIMATELY -5 VDC.

2. THE ADDRESS BITS ARE ROUTED FROM THE MICROCOMPUTER MODULE (J2) TO THE REMAINING LOGIC MODULES (J1, J3, AND J4) ALONG THE ADDRESS BUS. THE FOLLOWING IS AN ADDRESS BIT TO PIN NUMBER LIST:

AB00	A28	AB06	B29	AB11	B28
AB01	A27	AB07	B30	AB12	A32
AB02	A29	AB08	B31	AB13	A26
AB03	B26	AB09	B32	AB14	A25
AB04	A30	AB10	B27	AB15	B25
AB05	A31				

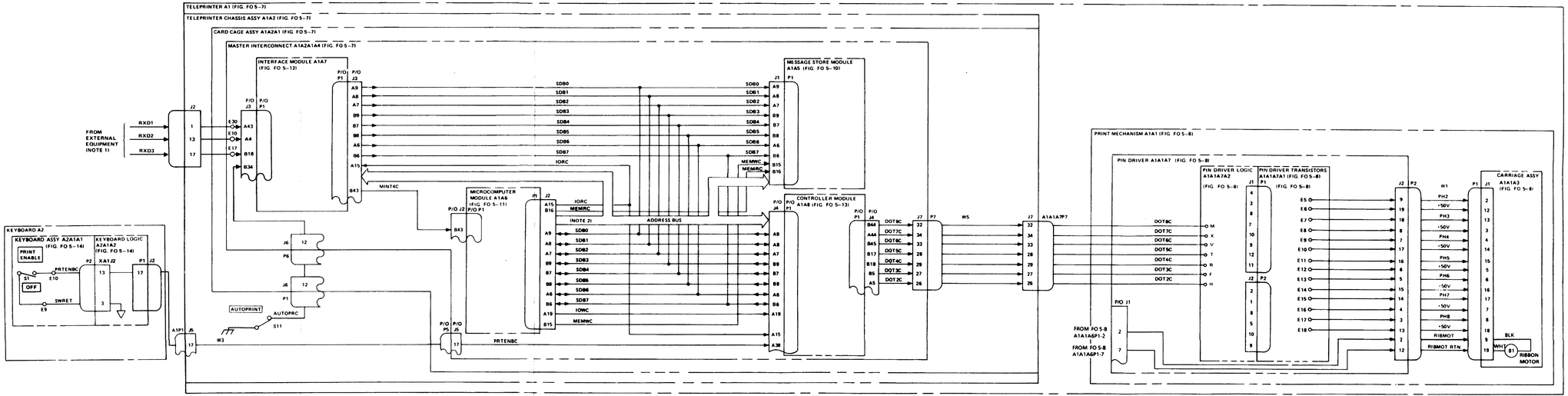


Figure FO 5-2. Receive Function, Signal Flow Diagram

GENERAL NOTES

A. IF NECESSARY, REFER TO FIGURE 5-13, FOR TROUBLESHOOTING AND PARAGRAPH 3-4, FOR FUNCTIONAL DESCRIPTION.

B. [ ] INDICATES FRONT PANEL MARKINGS.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

- CIRCUIT GROUND
- PULLUP
- TO
- FROM
- TEST POINT
- CHASSIS GROUND

SPECIFIC NOTES

1. THE ADDRESS BITS ARE ROUTED FROM THE MICROCOMPUTER MODULE (J2) TO THE REMAINING LOGIC MODULES (J1, J3, AND J4) ALONG THE ADDRESS BUS. THE FOLLOWING IS AN ADDRESS BIT TO PIN NUMBER LIST.

AB00	A28	AB06	B29	AB11	B28
AB01	A27	AB07	B30	AB12	A32
AB02	A29	AB08	B31	AB13	A26
AB03	B26	AB09	B32	AB14	A25
AB04	A30	AB10	B27	AB15	B25
AB05	A31				

2. THE TRANSMITTED SIGNAL, TXD3 FROM A1A7, IS A BIPOLAR SIGNAL WITH A LOGIC HIGH OF APPROXIMATELY +5 VDC AND A LOGIC LOW OF APPROXIMATELY -5 VDC.

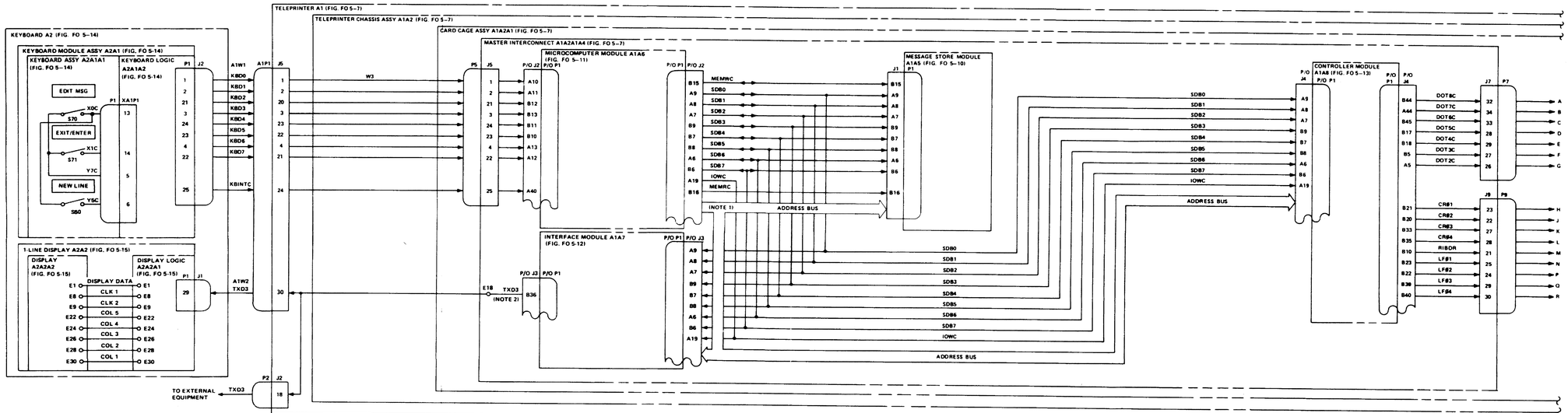


Figure FO 5-3. Compose/Edit Function, Signal Flow Diagram (Sheet 1 of 2)

Original

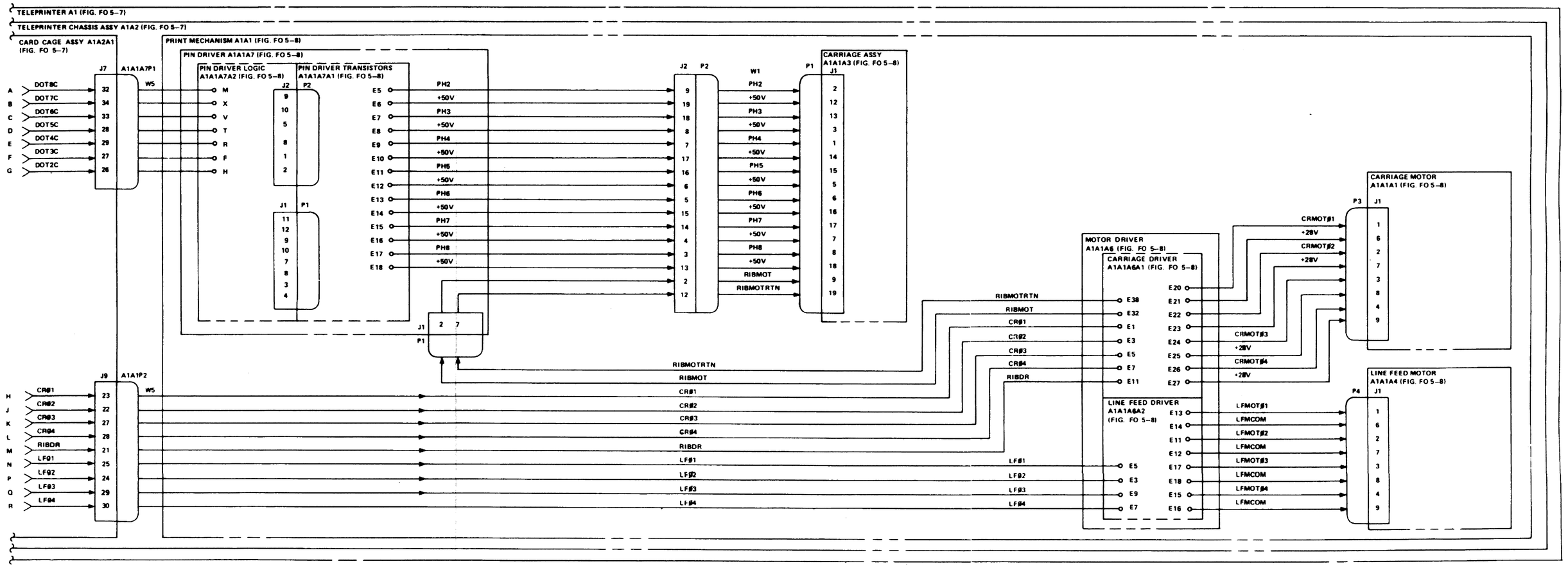


Figure FO 5-3. Compose/Edit Function, Signal Flow Diagram (Sheet 2 of 3)

GENERAL NOTES

A. IF NECESSARY, REFER TO FIGURE 5-8, FOR TROUBLESHOOTING AND PARAGRAPH 3-7, FOR FUNCTIONAL DESCRIPTION.

B. INDICATES FRONT PANEL MARKINGS.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

- CIRCUIT GROUND
- PULLUP
- TO
- FROM
- TEST POINT
- CHASSIS GROUND

SPECIFIC NOTES

1. THE SYSTEM DATA BUS IS BIDIRECTIONAL BOTH RECEIVING AND SENDING DATA OVER THE SAME LINES. IN THIS DIAGRAM IT IS SHOWN AS AN INPUT AND AN OUTPUT TO THE MICROCOMPUTER MODULE FOR CLARITY.

2. THE ADDRESS BITS ARE ROUTED FROM THE MICROCOMPUTER MODULE (J2) TO THE REMAINING LOGIC MODULES (J1, J3, AND J4) ALONG THE ADDRESS BUS. THE FOLLOWING IS AN ADDRESS BIT TO PIN NUMBER LIST.

AB00	A28	AB06	B29	AB11	B28
AB01	A27	AB07	B30	AB12	A32
AB02	A29	AB08	B31	AB13	A26
AB03	B26	AB09	B32	AB14	A25
AB04	A30	AB10	B27	AB15	B25
AB05	A31				

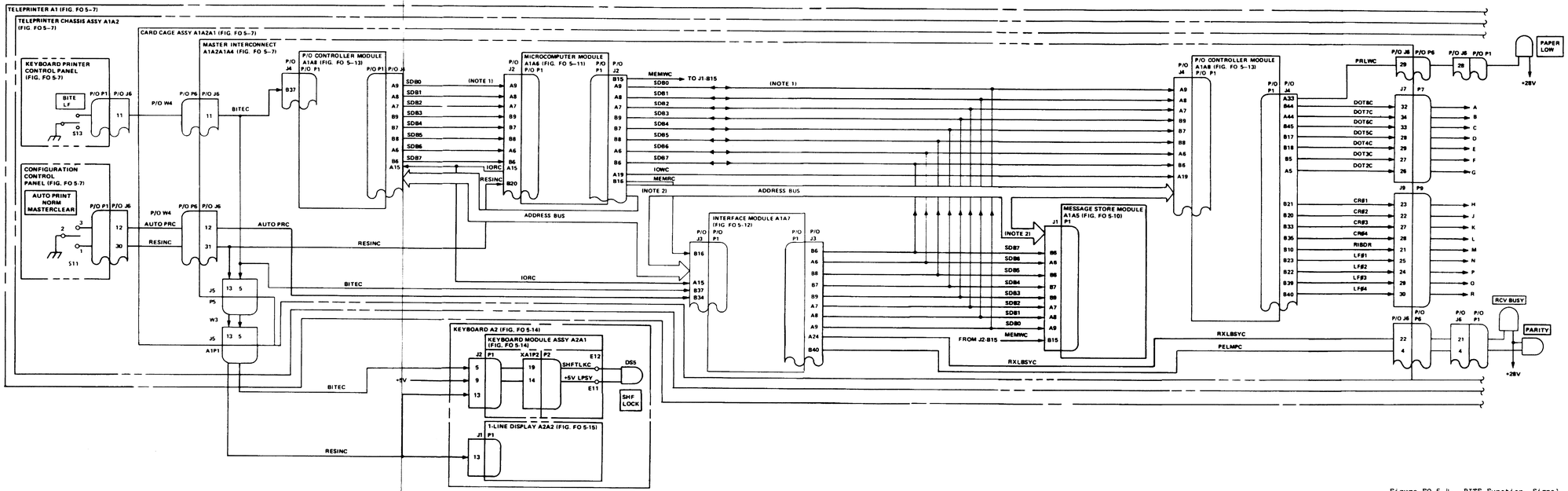


Figure FO 5-4. BITE Function, Signal Flow Diagram (Sheet 1 of 2)

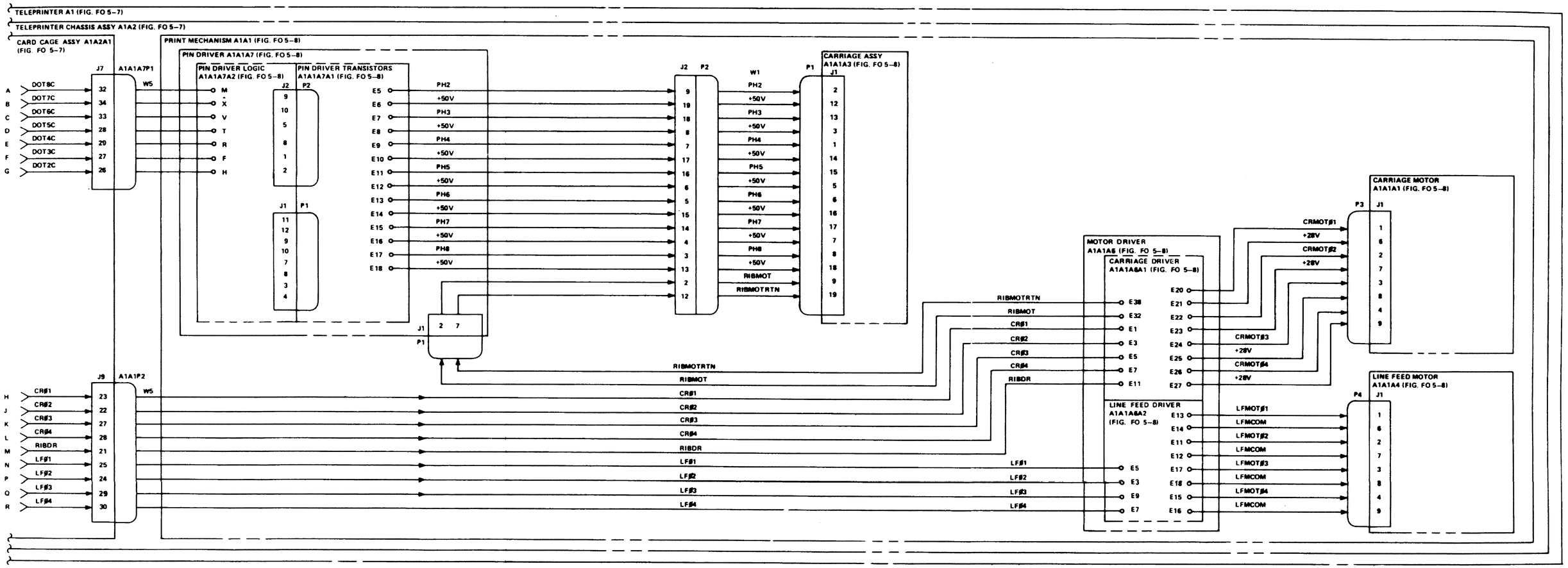


Figure FO 5-4. BITE Function, Signal Flow Diagram (Sheet 2 of 2)

GENERAL NOTES

A. ALL SWITCHES AND RELAY CIRCUITS ARE SHOWN IN OPERATING POSITIONS.

B. ▭ INDICATES FRONT PANEL MARKINGS.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

- CIRCUIT GROUND
- PULLUP
- TO
- FROM
- TEST POINT
- CHASSIS GROUND

SPECIFIC NOTES

1. MULTIPOSITION SWITCHES ARE SHOWN AS FOLLOWS:

REF. DES	POSITION SHOWN
S9	NONE
S10	2400
S11	NORM
S15	OFF (NOT USED)

2. SWITCHES S13 AND S14 ARE THREE-POSITION SWITCHES. THESE SWITCHES ARE SHOWN IN THE CENTER-LOCK POSITION, WHICH IS THE NORMAL POSITION.

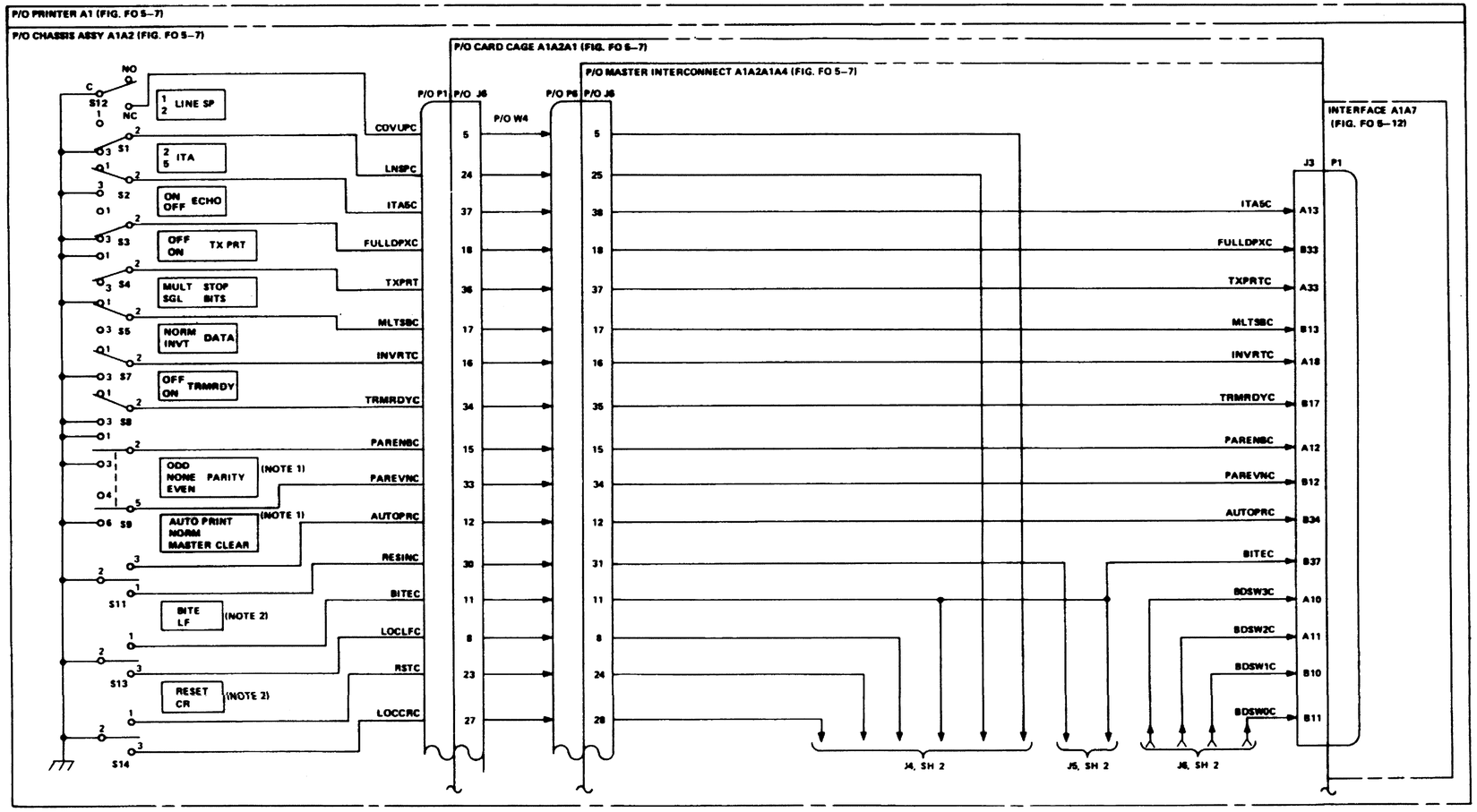


Figure FO 5-5. Keyboard-Printer, Control Diagram (Sheet 1 of 2)

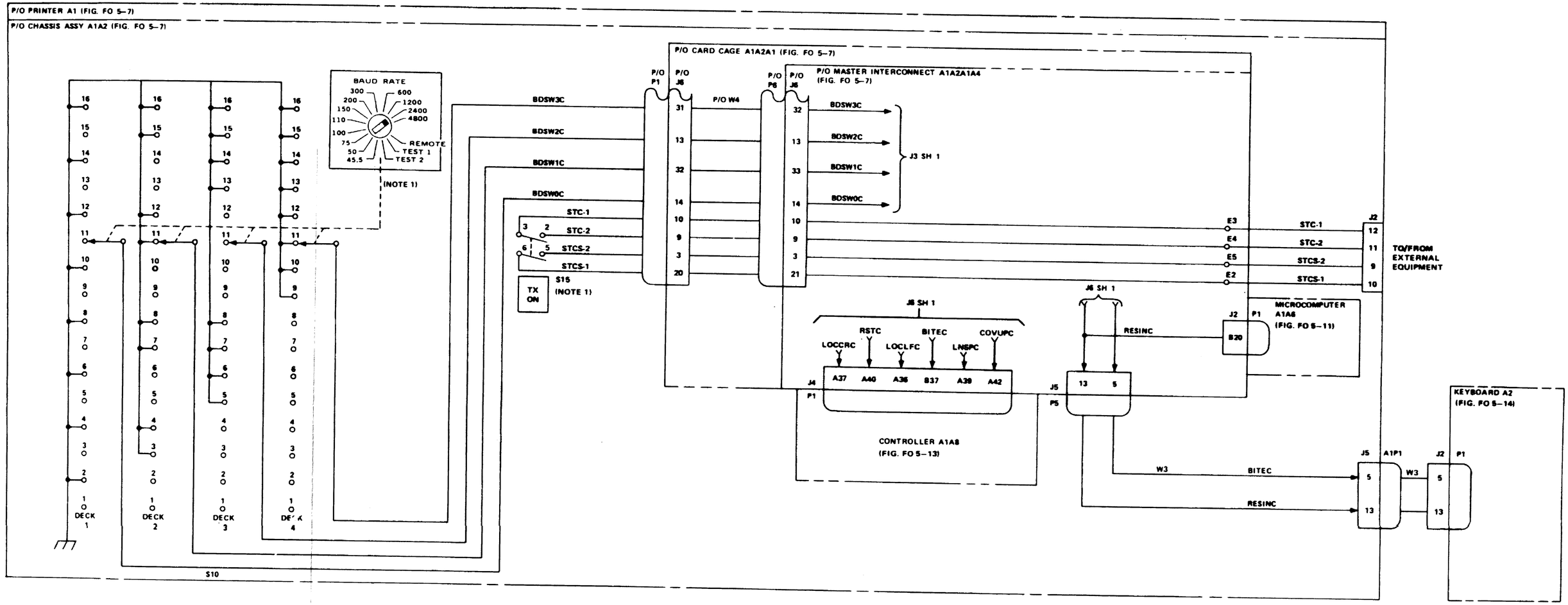


Figure FO 5-5. Keyboard-Printer, Control Diagram (Sheet 2 of 2)

GENERAL NOTES

A. INDICATES FRONT PANEL MARKINGS.

B. ALL SWITCHES ARE SHOWN IN THE OPERATING POSITIONS.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

- CIRCUIT GROUND
- PULLUP
- TO
- FROM
- TEST POINT
- CHASSIS GROUND

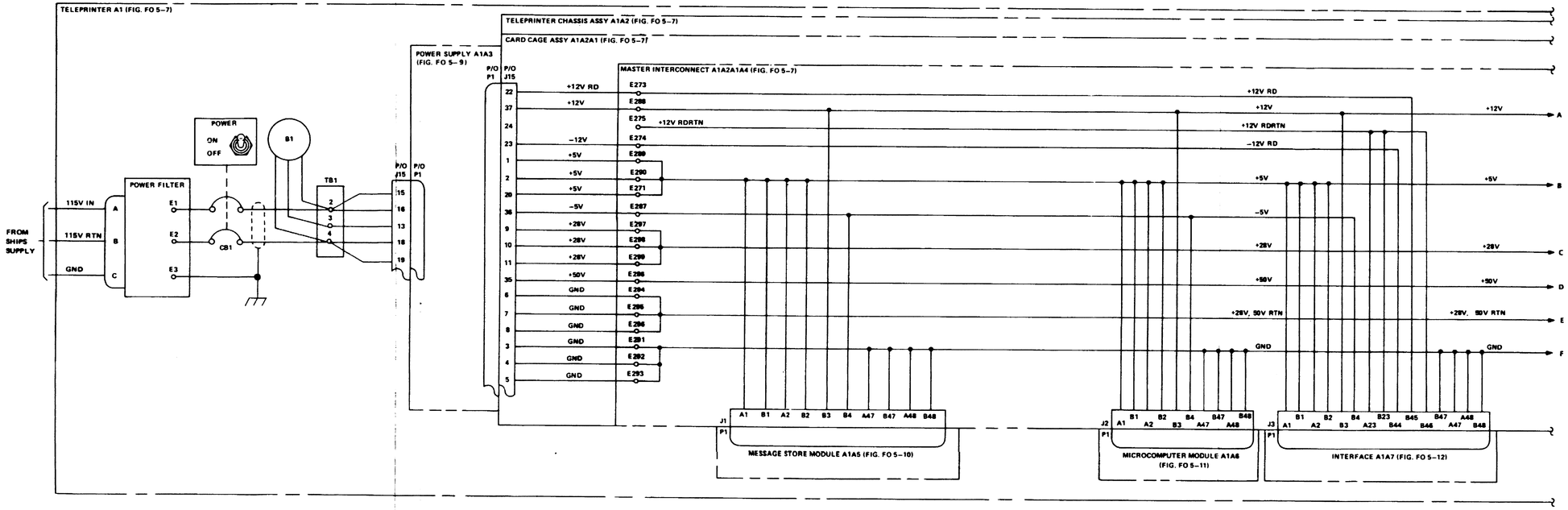


Figure FO 5-6. Keyboard-Printer, Power Distribution Diagram (Sheet 1 of 2)

SPECIFIC NOTES

1. FOR INDICATOR AND SPEAKER CONTROL SIGNALS SEE APPROPRIATE SCHEMATIC.

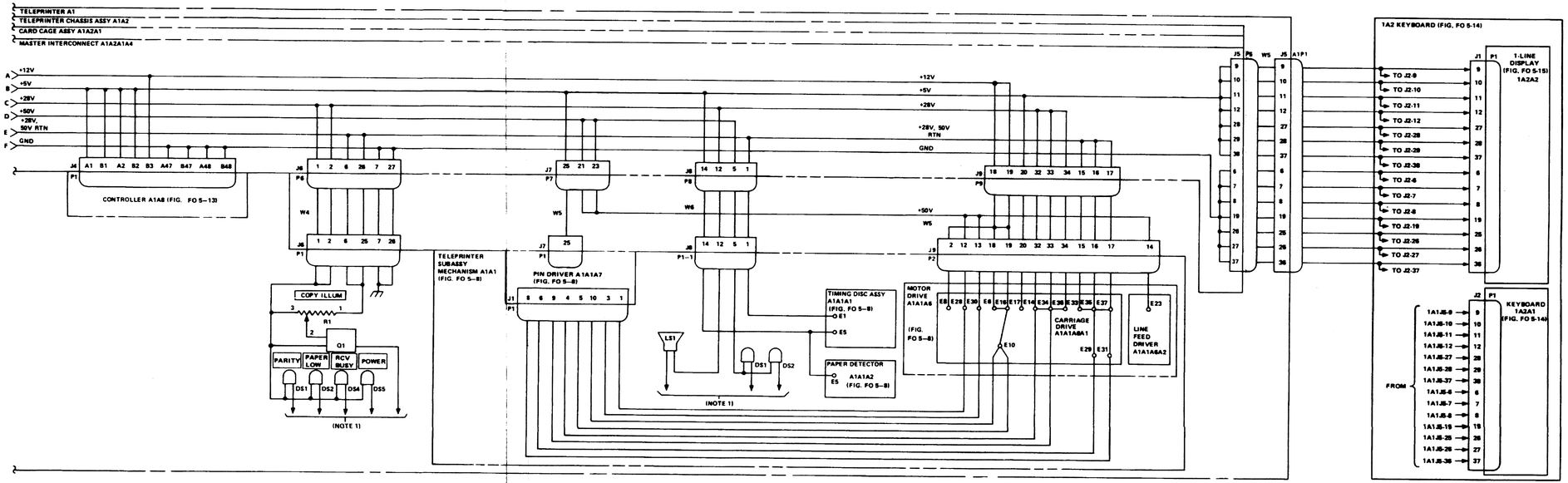


Figure FO 5-6. Keyboard-Printer, Power Distribution Diagram (Sheet 2 of 2)

Original

GENERAL NOTES

A. [ ] INDICATES FRONT PANEL MARKINGS.

B. ALL SWITCHES ARE SHOWN IN THE OPERATING POSITIONS.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

- CIRCUIT GROUND
- PULLUP
- TO
- FROM
- TEST POINT
- CHASSIS GROUND

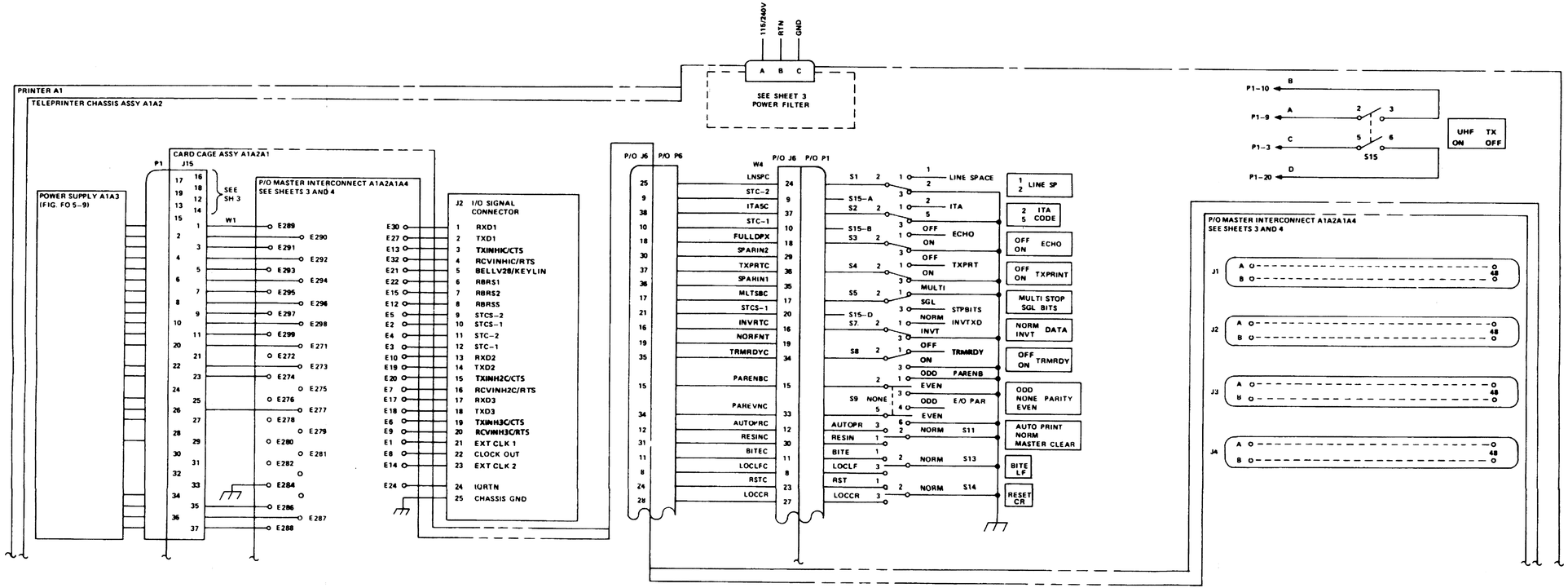
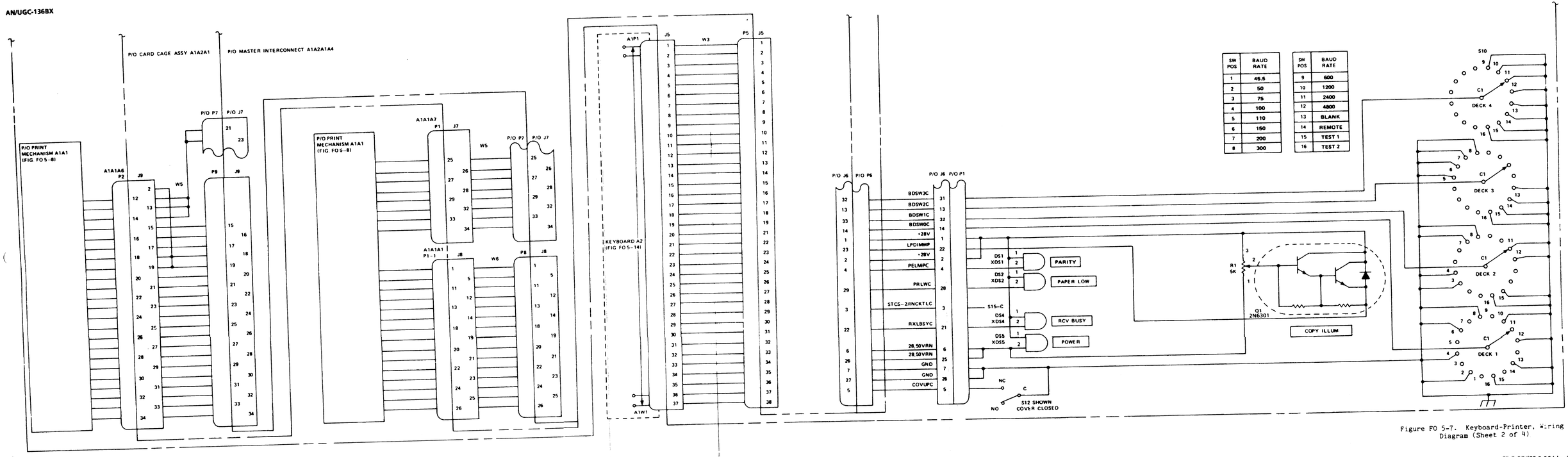


Figure FO 5-7. Keyboard-Printer, Wiring Diagram (Sheet 1 of 4)



SW POS	BAUD RATE
1	45.5
2	50
3	75
4	100
5	110
6	150
7	200
8	300

SW POS	BAUD RATE
9	600
10	1200
11	2400
12	4800
13	BLANK
14	REMOTE
15	TEST 1
16	TEST 2

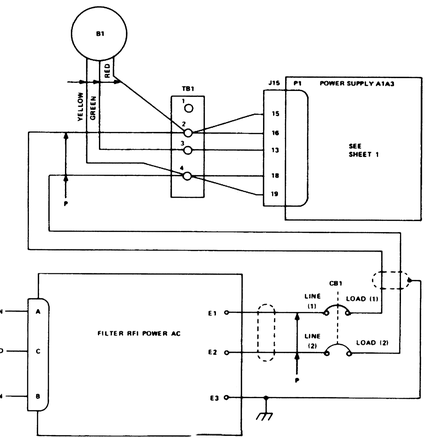
Figure FO 5-7. Keyboard-Printer, Wiring Diagram (Sheet 2 of 4)

SPECIFIC NOTES

1. THE +5 VDC IS THE SOURCE VOLTAGE FOR THE TTL LOGIC. IT IS DEVELOPED IN THE POWER SUPPLY A1A3 AND ROUTED TO ALL LOGIC CIRCUITS. THE +5 VDC SOURCE FROM THE POWER SUPPLY IS CONNECTED TO TERMINALS E271, E289, E290, E300, AND E301.

2. THE CHASSIS GROUND CONNECTION TO THE POWER SUPPLY A1A3 IS AT TERMINALS E272, E284, E285, E291, E292, AND E293.

3. THE +28 VDC AND +50 VDC RETURN LINE CONNECTION TO THE POWER SUPPLY A1A3 IS AT TERMINALS E294, E295, AND E296.



MASTER INTERCONNECT WIRE RUN LIST

FROM	TO	MNEMONIC	FROM	TO	MNEMONIC
J1-A1	SEE NOTE 1	+5V	J2-A8	J1-A8, J3-A8, J4-A8	SDB1
J1-A2	SEE NOTE 1	+5V			
J1-A3	E283	BAT2	J2-A9	J1-A9, J3-A9, J4-A9	SDB0
J1-A4	J2-A17	POCC			
J1-A6	J2-A6	SDB6	J2-A10	J5-1	KBD0
J1-A7	J2-A7	SDB2	J2-A11	J5-2	KBD1
J1-A8	J2-A8	SDB1	J2-A12	J5-22	KBD7
J1-A9	J2-A9	SDB0	J2-A13	J5-4	KBD6
J1-A14	J2-A14	Ø2TTL	J2-A14	J3-A14	Ø2TTL
J1-A15	J2-A15	IORC	J2-A15	J1-A15, J3-A15, J4-A15	IORC
J1-A19	J2-A19	IOWC			
J1-A25	J2-A25	AB14	J2-A16	J2-B21	INTE
J1-A26	J2-A26	AB13	J2-A17	J3-A17, J4-A17	POCC
J1-A27	J2-A27	AB01	J2-A19	J1-A19, J3-A19, J4-A19	IOWC
J1-A28	J2-A28	AB00			
J1-A29	J2-A29	AB02	J2-A20	J2-A22	QQ3C
J1-A30	J2-A30	AB04	J2-A22	J2-A20	WQ3C
J1-A31	J2-A31	AB05	J2-A23	J3-A3, J4-B38	SHMSK
J1-A32	J2-A32	AB12	J2-A25	J1-A25, J3-A25, J4-A25	AB14
J1-A47	SEE NOTE 2	GND			
J1-A48	SEE NOTE 2	GND	J2-A26	J1-A26, J3-A26, J4-A26	AB13
J1-B1	SEE NOTE 1	+5V			
J1-B2	SEE NOTE 1	+5V	J2-A27	J1-A27, J3-A27, J4-A28	AB01
J1-B3	E288	+12V			
J1-B4	E287	-5V	J2-A28	J1-A28, J3-A28, J4-A28	AB00
J1-B6	J2-B6	SDB7			
J1-B7	J2-B7	SDB4	J2-A29	J1-A29, J3-A29, J4-A29	AB02
J1-B8	J2-B8	SDB5			
J1-B9	J2-B9	SDB3	J2-A30	J1-A30, J3-A30, J4-A30	AB04
J1-B15	J2-B15	MEMWC			
J1-B16	J2-B16	MEMRC	J2-A31	J1-A31, J3-A31, J4-A31	AB05
J1-B25	J2-B25	AB15			
J1-B26	J2-B26	AB03	J2-A32	J1-A32, J3-A32, J4-A32	AB12
J1-B27	J2-B27	AB10			
J1-B28	J2-B28	AB11	J2-A33	J5-32	CEACT
J1-B29	J2-B29	AB06	J2-A34	J5-14	EOL
J1-B30	J2-B30	AB07	J2-A35	E12	RBRSS
J1-B31	B2-B31	AB08	J2-A36	J5-15	TXACT
J1-B32	J2-B32	AB09	J2-A40	J5-25	KBINTC
J1-B42	J2-A23	SHMSK	J2-A41	J4-B19	MINT7C
J1-B47	SEE NOTE 2	GND	J2-A43	J4-A43	RSI3C
J1-B48	SEE NOTE 2	GND	J2-A47	SEE NOTE 2	GND
			J2-A48	SEE NOTE 2	GND
J2-A1	SEE NOTE 1	+5V	J2-B1	SEE NOTE 1	+5V
J2-A2	SEE NOTE 1	+5V	J2-B2	SEE NOTE 1	+5V
J2-A3	J4-A3	115/POWDN	J2-B3	E288	+12V
J2-A6	J1-A6, J3-A6, J4-A6	SDB6	J2-B4	E287	-5V
J2-A7	J1-A7, J3-A7, J4-A7	SDB2	J2-B5	J6-B14, E281	PRDW/+10VRD
			J2-B6	J1-B6, J3-B6, J4-B6	SDB7

MASTER INTERCONNECT WIRE RUN LIST

FROM	TO	MNEMONIC	FROM	TO	MNEMONIC
J2-B7	J1-B7, J3-B7 J4-B7	SDB4	J3-A10	J6-32	BDSW3C
			J3-A11	J6-13	BDSW2C
J2-B8	J1-B8, J3-B8, J4-B8	SDB5	J3-A12	J6-15	PARENWBCC
			J3-A13	J6-38	IT45C
J2-B9	J1-B9, J3-B9, J4-B9	SDB3	J3-A14	J2-A14	Ø2TTL
			J3-A15	J2-A15	IORC
J2-B10	J5-23	KBD5	J3-A16	J4-A20, J4-A21, E282	BAT1/ 10RDRN
J2-B11	J5-24	KBD4			
J2-B12	J5-21	KBD2	J3-A17	J2-A17	POCC
J2-B13	J5-3	KBD3	J3-A18	J6-16	INVRTC
J2-B15	J1-B15, J3-B15, J4-B15	MEMWC	J3-A19	J2-A19	IOWC
			J3-A20	E11	RXDCL2
J2-B16	J1-B16, J3-B16, J4-B16	MEMRC	J3-A21	E16	RXDCL1
			J3-A22	E1	EXT CLK 1
J2-B20	J5-13, J6-31	RESINC	J3-A23	E275, J3-B23, J3-B46	+12, 8ORDRN
J2-B21	J2-A16	INTE			
J2-B25	J1-B25, J3-B25, J4-B25	AB15	J3-A24	J6-22	RXLBSYC
			J3-A25	J2-A25	AB14
J2-B26	J1-B26, J3-B26, J4-B26	AB03	J3-A26	J2-A26	AB13
			J3-A27	J2-A27	AB01
J2-B27	J1-B27, J3-B27, J4-B27	AB10	J3-A28	J2-A28	AB00
			J3-A29	J2-A29	AB02
J2-B28	J1-B28, J3-B28, J4-B28	AB11	J3-A30	J2-A30	AB04
			J3-A31	J2-A31	AB05
J2-B29	J1-B29, J3-B29, J4-B29	AB06	J3-A32	J2-A32	AB12
			J3-A33	J6-37	TXPRTC
J2-B30	J1-B30, J3-B30, J4-B30	AB07	J3-A34	E22	RBRS1
		J3-A35	E15	RBRS2	J3-B34
J2-B31	J1-B31, J3-B31, J4-B31	AB08	J3-A36	E21	BELLV28/ KEYLIN
J2-B32	J1-B32, J3-B32 J4-B32	AB09	J3-A37	E5, J6-3	STCS-2
			J3-A38	E13	TXINH1C
J2-B33	J5-31	RXUNP	J3-A39	J2-B35	PERR
J2-B34	J4-B34	OUTA4	J3-A40	E27	TXD1
J2-B35	J3-A39	PERR	J3-A41	E20	TXINH2C
J2-B41	J4-B41	MINT3C	J3-A43	E30	RXD1
J2-B42	J3-B41	MINT5C	J3-A44	E8	CLKOUT
J2-B43	J3-B43	MINT4C	J3-A45	E7	RTS/ RCVINH2C
J2-B47	SEE NOTE 2	GND			
J2-B48	SEE NOTE 2	GND	J3-A46	E24	IORTN
			J3-A47	SEE NOTE 2	GND
J3-A1	SEE NOTE 10	+5V	J3-A48	SEE NOTE 2	GND
J3-A2	SEE NOTE 1	+5V			
J3-A3	J2-A23	SHMSK	J3-B1	SEE NOTE 1	+5V
J3-A4	E10	RXD2	J3-B2	SEE NOTE 2	+5V
J3-A5	E19	TXD2	J3-B3	E288	+12V
J3-A6	J2-A6	SDB6	J3-B4	E287	-5V
J3-A7	J2-A7	SDB2	J3-B6	J2-B6	SDB7
J3-A8	J2-A8	SDB1	J3-B7	J2-B7	SDB4
J3-A9	J2-A9	SDB0	J3-B8	J2-B8	SDB5

MASTER INTERCONNECT WIRE RUN LIST

FROM	TO	MNEMONIC	FROM	TO	MNEMONIC
J3-B9	J2-B9	SDB3	J4-A6	J2-A6	SDB6
J3-B10	J6-33	BDSW1C	J4-A7	J2-A7	SDB2
J3-B11	J6-14	BDSW0C	J4-A8	J2-A8	SDB1
J3-B12	J6-34	PAREVNC	J4-A9	J2-A9	SDB0
J3-B13	J6-17	MLTSBC	J4-A11	J8-22	BRKC
J3-B14	J2-B5, E281	PRDW/ +10VRD	J4-A12	J8-11	BRK12
			J4-A13	J8-24	BRKRTN
J3-B15	J2-B15	MEMWC	J4-A14	J8-26	MPCRTN
J3-B16	J2-B16	MEMRC	J4-A15	J2-A15	IORC
J3-B17	J6-35	TRMRDYC	JR-A16	J6-19	NORFNT
J3-B18	J5-16, E-17	RXD3	J4-A17	J2-A17	POCC
J3-B19	E28	TXDCL2	J4-A19	J2-A19	IOWC
J3-B20	E29	TXDCL1	J4-A20	J4-A21, J3-A16, E282	BAT1/ 10RDRN
J3-B22	E276	+80VRD			
J3-B23	E275, J3-A23, J3-B46	+12, 8ORDRN	J4-A21	J4-A20, J3-A16, E282	BAT1/ 10RDRN
J3-B24	E278	-80VRD	J4-A25	J2-A25	AB14
J3-B25	J2-B25	AB15	J4-A26	J2-A26	AB13
J3-B26	J1-B26, J2-B26, J4-B26	ABO3	J4-A27	J2-A27	ABO1
			J4-A28	J2-A28	ABO0
J3-B27	J2-B27	AB10	J4-A29	J2-A29	ABO2
J3-B28	J2-B28	AB11	J4-A30	J2-A30	ABO4
J3-B29	J2-B29	AB06	J4-A31	J2-A31	ABO5
J3-B30	J2-B30	AB07	J4-A32	J2-A32	AB12
J3-B31	J2-B31	AB08	J4-A33	J6-29	PRLWC
J3-B32	J2-B32	AB09	J4-A36	J6-8	LOCLFC
J3-B33	J6-18	FULLDPX	J4-A37	J6-28	LOCCRC
J3-B34	J6-12	AUTOPRC	J4-A38	J5-17	PRTENB
J3-B35	J5-18	BREAKC	J4-A39	J6-25	LNSPC
J3-B36	J5-30, E18	TXD3	J4-A40	J6-24	RSTC
J3-B37	J6-11	BITEC	J4-A42	J6-5	COVUPC
J3-B38	E14	EXT CLK 2	J4-A43	J2-A43	RSI3C
J3-B39	E32	RTS/ RCVINH1C	J4-A44	J7-34	DOT7C
			J4-A45	J9-31	LFHLDC
J3-B40	J6-4	PELMPC	J4-A46	E277	OVRTEMP
J3-B41	J2-B42	MINT5C	J4-A47	SEE NOTE 2	GND
J3-B42	J5-36, E9	RTS/ RCVINH3C	J4-A48	SEE NOTE 2	GND
J3-B43	J2-B43	MINT4C	J4-B1	SEE NOTE 1	+5V
J3-B44	E274	-12VRD	J4-B2	SEE NOTE 1	+5V
J3-B45	E273	+12VRD	J4-B3	E288	+12V
J3-B46	E275, J3-A23, J3-B23	+12, 8ORDRN	J4-B4	J8-19	PHDFC
			J4-B5	J7-27	DOT3C
J3-B47	SEE NOTE 2	GND	J4-B6	J2-B6	SDBV7
J3-B48	SEE NOTE 2	GND	J4-B7	J2-B7	SDB4
			J4-B8	J2-B8	SDB5
J4-A1	SEE NOTE 1	+5V	J4-B9	J2-B9	SDB3
J4-A2	SEE NOTE 1	+5V	J4-B11	J8-21	RIBDR
J4-A3	J2-A3	115/POWDN	J4-B12	J8-13	MOTC
J4-A4	J8-20	SYNCC	J4-B13	J8-23	MPC12
J4-A5	J7-26	DOT2C	J4-B13	J8-23	PAPLOWC

Figure FO 5-7. Keyboard-Printer, Wiring Diagram (Sheet 3 of 4)

MASTER INTERCONNECT WIRE RUN LIST

FROM	TO	MNEMONIC	FROM	TO	MNEMONIC
J4-B14	J8-25	EOLAC	J4-B40	J9-30	LFO4
J4-B15	J2-B15	MEMWC	J4-B41	J2-B41	MINT3C
J4-B16	J2-B16	MEMRC	J4-B42	J7-30	DOT9C
J4-B17	J7-28	DOT5C	J4-B43	J7-31	DOT1C
J4-B18	J7-29	DOT4C	J4-B44	J7-32	DOT8C
J4-B19	J2-A41	MINT7C	J4-B45	J7-33	DOT6C
J4-B20	J9-22	CRO2	J4-B47	SEE NOTE 2	GND
J4-B21	J9-23	CRO1	J4-B48	SEE NOTE 2	GND
J4-B22	J9-24	LFO2			
J4-B23	J9-25	LFO1	J5-1	J2-A10	KBD0
J4-B24	J9-26	HISPC	J5-2	J2-A11	KBD1
J4-B25	J2-B25	AB15	J5-3	J2-B13	KBD3
J4-B26	J1-B26, J2-B26, J3-B26	AB03	J5-4	J2-A13	KBD6
			J5-5	J6-11	BITEC
J4-B27	J2-B27	AB10	J5-6	SEE NOTE 2	GND
J4-B28	J2-B28	AB11	J5-7	SEE NOTE 2	GND
J4-B29	J2-B29	AB06	J5-8	SEE NOTE 2	GND
J4-B30	J2-B30	AB07	J5-9	SEE NOTE 1	+5V
J4-B31	J2-B31	AB08	J5-10	SEE NOTE 1	+5V
J4-B32	J2-B32	AB09	J5-11	SEE NOTE 1	+5V
J4-B33	J9-27	CRO3	J5-12	SEE NOTE 1	+5V
J4-B34	J2-B34	OUTA4	J5-13	J2-B20, J6-31	RESINC
J4-B35	J9-28	CRO4	J5-14	J2-A34	EOL
J4-B36	J2-B36	EOLA	J5-15	J2-A36	TXACT
J4-B37	J6-11	BITEC	J5-16	J3-B18	RXD3
J4-B38	J2-A23	SHMSK	J5-17	J4-A38	PRTENB
J4-B39	J9-29	LFO3	J5-18	J3-B35	BREAKC

MASTER INTERCONNECT WIRE RUN LIST

FROM	TO	MNEMONIC	FROM	TO	MNEMONIC
J5-19	SEE NOTE 2	GND	J6-33	J3-B10	BDSW1C
J5-21	J2-B12	KBD2	J6-34	J3-B12	PAREVNC
J5-22	J2-A12	KBD7	J6-35	J3-B17	TRMRDYC
J5-23	J2-B10	KBD5	J6-36	N/C	SPAR1
J5-24	J2-B11	KBD4	J6-37	J3-A33	TXPRTC
J5-25	J2-A40	KBINTC	J6-38	J3-A13	ITA5C
J5-26	SEE NOTE 2	GND			
J5-27	SEE NOTE 2	GND	J7-1	SEE NOTE 2	GND
J5-28	SEE NOTE 1	+5V	J7-2	SEE NOTE 2	GND
J5-29	SEE NOTE 1	+5V	J7-3	SEE NOTE 3	28, 50 RN
J5-30	J3-B36, E18	TXD3	J7-4	SEE NOTE 3	28, 50 RN
J5-31	J2-B33	RXUNP	J7-5	SEE NOTE 2	GND
J5-32	J2-A33	CEACT	J7-6	SEE NOTE 3	28, 50 RN
J5-33	J3-A42, E6	TXINH3C	J7-7	SEE NOTE 3	28, 50 RN
J5-36	J3-B42, E9	RTS/ RCVINH3C	J7-8	SEE NOTE 2	GND
			J7-9	SEE NOTE 2	GND
J5-37	SEE NOTE 2	GND	J7-10	SEE NOTE 2	GND
J5-38	SEE NOTE 1	+5V	J7-11	SEE NOTE 2	GND
			J7-12	SEE NOTE 2	GND
J6-1	E297	+28V	J7-13	SEE NOTE 2	GND
J6-2	E297	+28V	J7-14	SEE NOTE 2	GND
J6-3	E5, J3-A37	STCS-2	J7-15	SEE NOTE 2	GND
J6-4	J3-B40	PELMPC	J7-16	SEE NOTE 2	GND
J6-5	J4-A42	COVUPC	J7-17	SEE NOTE 2	GND
J6-6	SEE NOTE 3	28,50 RN	J7-18	E288	+12V
J6-7	SEE NOTE 2	GND	J7-19	SEE NOTE 1	+5V
J6-8	J4-A36	LOCLFC	J7-20	E298	+28V
J6-9	E4	STC-2	J7-21	E286	+50V
J6-10	E3	STC-1	J7-22	E288	+12V
J6-11	J3-B37, J4-B37, J5-5	BITEC	J7-23	E286	+50V
			J7-24	E298	+28V
J6-12	J3-B34	AUTOPRC	J7-25	SEE NOTE 1	+5V
J6-13	J3-A11	BDSW2C	J7-26	J4-A5	DOT2C
J6-14	J3-B11	BDSW0C	J7-27	J4-B5	DOT3C
J6-15	J3-A12	PARENBC	J7-28	J4-B18	DOT5C
J6-16	J3-A18	INVRTC	J7-29	J4-B17	DOT4C
J6-17	J3-B13	MLTSBC	J7-30	J4-B42	DOT9C
J6-18	J3-B33	FULLDPX	J7-31	J4-B43	DOT1C
J6-19	J4-A16	NORFNT	J7-32	J4-B44	DOT8C
J6-21	E2	STCS-1	J7-33	J4-A45	DOT6C
J6-22	J3-A24	RXLBSYC	J7-34	J4-A44	DOT7C
J6-23	J8-18	LPDIMWP			
J6-24	J4-A40	RSTC	J8-1	SEE NOTE 2	GND
J6-25	J4-A39	LNSPC	J8-2	SEE NOTE 2	GND
J6-26	SEE NOTE 3	28,50 RN	J8-3	SEE NOTE 2	GND
J6-27	SEE NOTE 2	GND	J8-4	SEE NOTE 2	GND
J6-28	J4-A37	LOCCRC	J8-5	SEE NOTE 3	28, 50 RN
J6-29	J4-A33	PRLWC	J8-6	SEE NOTE 2	GND
J6-30	N/C	SPAR2	J8-7	SEE NOTE 2	GND
J6-31	J2-B20	RESINC	J8-8	SEE NOTE 2	GND
J6-32	J3-A10	BDSW3C	J8-9	SEE NOTE 2	GND

MASTER INTERCONNECT WIRE RUN LIST

FROM	TO	MNEMONIC	FROM	TO	MNEMONIC
J8-10	SEE NOTE 2	GND	J9-34	E299	+28V
J8-11	J4-A12	BRK12			
J8-12	E298	+28V	E1	J3-A22	EXT CLK 1
J8-13	J4-B12	MPC12	E2	J6-21	STCS-1
J8-14	SEE NOTE 1	+5V	E3	J6-10	STC-1
J8-15	SEE NOTE 1	+5V	E4	J6-9	STC-2
J8-16	SEE NOTE 1	+5V	E5	J3-A37, J6-35	STCS-2
J8-17	SEE NOTE 1	+5V	E6	J5-33	TXINH3C
J8-18	J6-23	LPDIMWP	E7	J3-A45	RTS/ RCVINH2C
J8-19	J4-B4	PHDFC			
J8-20	J4-A4	SYNCC	E8	J3-A44	CLKOUT
J8-21	J4-B11	MOTC	E9	J3-B42, J5-36	RTS/ RCVINH3C
J8-22	J4-A11	BRKC			
J8-23	J4-B13	PAPLOWC	E10	J3-A4	RXD2
J8-24	J4-A13	BRKRTN	E11	J3-A20	RXDCL2
J8-25	J4-B14	EOLAC	E12	J2-A35	RBRSS
J8-26	J4-A14	MPCRTN	E13	J3-A38	TXINH1C
			E14	J3-B38	EXT CLK 2
J9-1	SEE NOTE 2	GND	E15	J2-A35	RBRS2
J9-2	SEE NOTE 2	GND	E16	J3-A21	RXDCL1
J9-3	SEE NOTE 2	GND	E17	J3-B18, J5-16	RXD3
J9-4	SEE NOTE 2	GND	E18	J3-B36, J5-30	TXD3
J9-5	SEE NOTE 2	GND	E19	J3-A5	TXD2
J9-6	SEE NOTE 2	GND	E20	J3-A41	TXINH2C
J9-7	SEE NOTE 2	GND	E21	J3-A36	BELLV28/ KEYLIN
J9-8	SEE NOTE 2	GND			
J9-9	SEE NOTE 2	GND	E22	J3-A34	RBRS1
J9-10	SEE NOTE 2	GND	E24	J3-A46	IORTN
J9-11	SEE NOTE 2	GND	E25	E305	+60VRD
J9-12	SEE NOTE 2	GND	E26	E302	+60VRDRN
J9-13	SEE NOTE 2	GND	E27	J3-A40	TXD1
J9-14	SEE NOTE 2	GND	E28	J3-B19	TXDCL2
J9-15	SEE NOTE 3	28, 50 RN	E29	J3-B20	TXDCL1
J9-16	SEE NOTE 3	28, 50 RN	E30	J3-A43	RXD1
J9-17	SEE NOTE 3	28, 50 RN	E32	J3-B39	RTS/ RCVINH1C
J9-18	E288	+12V			
J9-19	E288	+12V			
J9-20	SEE NOTE 1	+5V	E271	SEE NOTE 1	+5V
J9-21	J4-B10	RIBDR	E272	SEE NOTE 2	GND
J9-22	J4-B20	CRO2	E273	J3-B45	+12VRD
J9-23	J4-B21	CRO1	E274	J3-B44	-12VRD
J9-24	J4-B22	LFO2	E275	J3-A23, J3-B23, J3-B46	+12, 80 RDRN
J9-25	J4-B23	LFO1			
J9-26	J4-B24	HISPC	E276	J3-B22	+80VRD
J9-27	J4-B33	CRO3	E277	J4-A46	OVRTEMP
J9-28	J4-B35	CRO4	E278	J3-B24	-80VRD
J9-29	J4-B39	LFO3	E279	E303	+60VRDRNP
J9-30	J4-B40	LFO4	E280	E304	+60VRDP
J9-31	J4-A45	LFHLDC	E281	J2-B5, J3-B14	PRDW/ +10VRD
J9-32	E299	+28V			
J9-33	E299	+28V			

MASTER INTERCONNECT WIRE RUN LIST

FROM	TO	MNEMONIC
E282	J3-A16, J4-A20, J4-A21	BAT1/ 10RDRN
E283	J1-A3	BAT2
E284	SEE NOTE 2	GND
E285	SEE NOTE 2	GND
E286	J7-21, J7-23	+50V
E287	J1-B4, J2-B4, J3-B4	-5V
E288	J1-B3, J2-B3, J3-B3, J4-B3, J7-22, J7-18, J9-18, J9-19	+12V
E289	SEE NOTE 1	+5V
E290	SEE NOTE 1	+5V
E291	SEE NOTE 2	GND
E292	SEE NOTE 2	GND
E293	SEE NOTE 2	GND
E294	SEE NOTE 3	28, 50 RN
E295	SEE NOTE 3	28, 50 RN
E296	SEE NOTE 3	28, 50 RN
E297	J6-1, J6-2	+28V
E298	J7-20, J7-24, J8-12	+28V
E299	J9-32, J9-33, J9-34	+28V
E300	SEE NOTE 1	+5V
E301	SEE NOTE 1	+5V
E302	E26	+60VRDRN
E303	E279	+60VRDRNP
E304	E280	+60VRDP
E305	E25	+60VRD

Figure FO 5-7. Keyboard-Printer, Wiring Diagram (Sheet 4 of 4)

GENERAL NOTES

UNLESS OTHERWISE SPECIFIED:

A. RESISTANCE VALUES ARE IN OHMS.

B. CAPACITANCE VALUES ARE IN MICROFARADS.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

CIRCUIT GROUND

PULLUP

TO

FROM

TEST POINT

CHASSIS GROUND

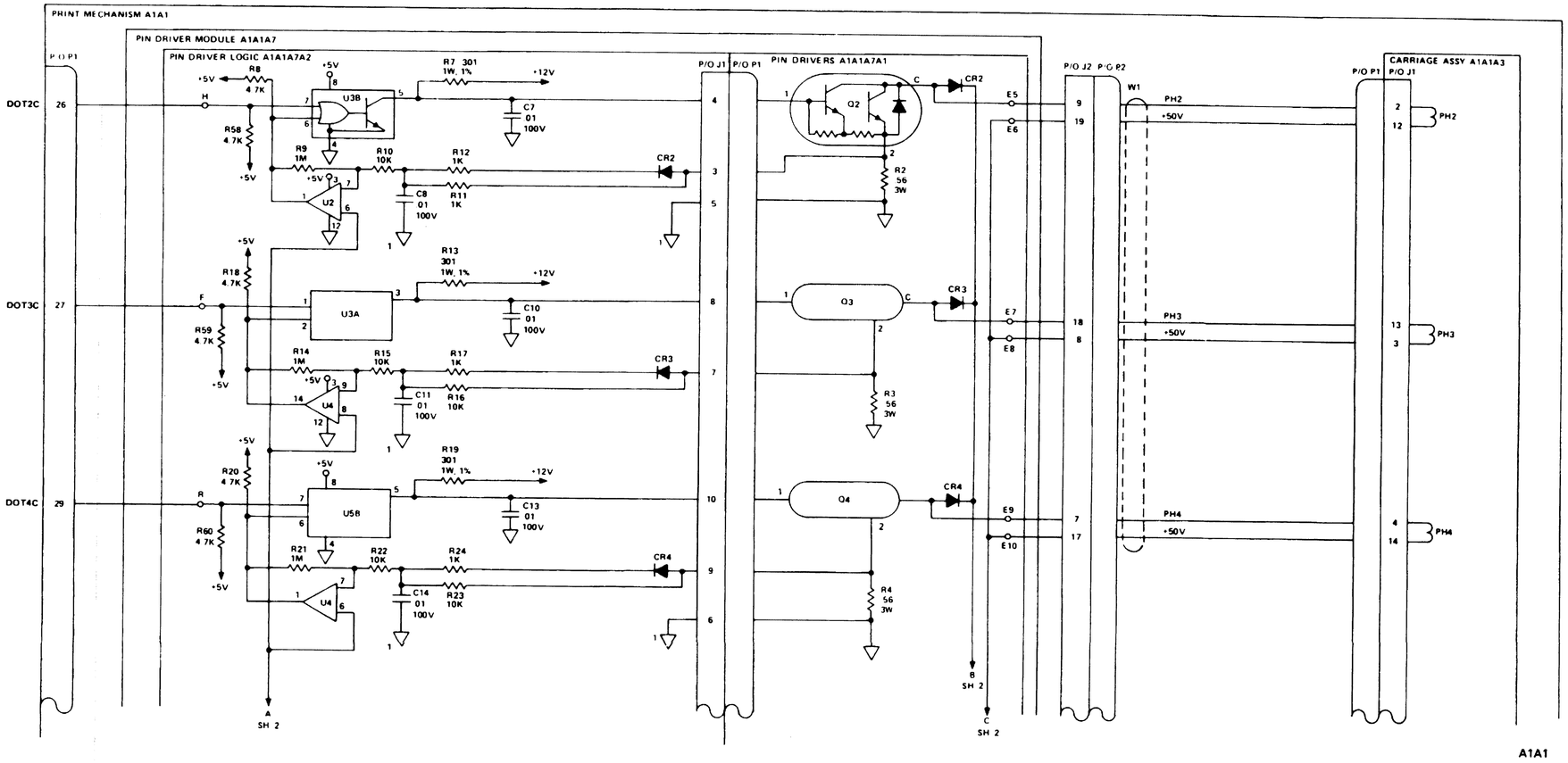


Figure FO 5-8. Print Mechanism (A1A1), Schematic Diagram (Sheet 1 of 7)

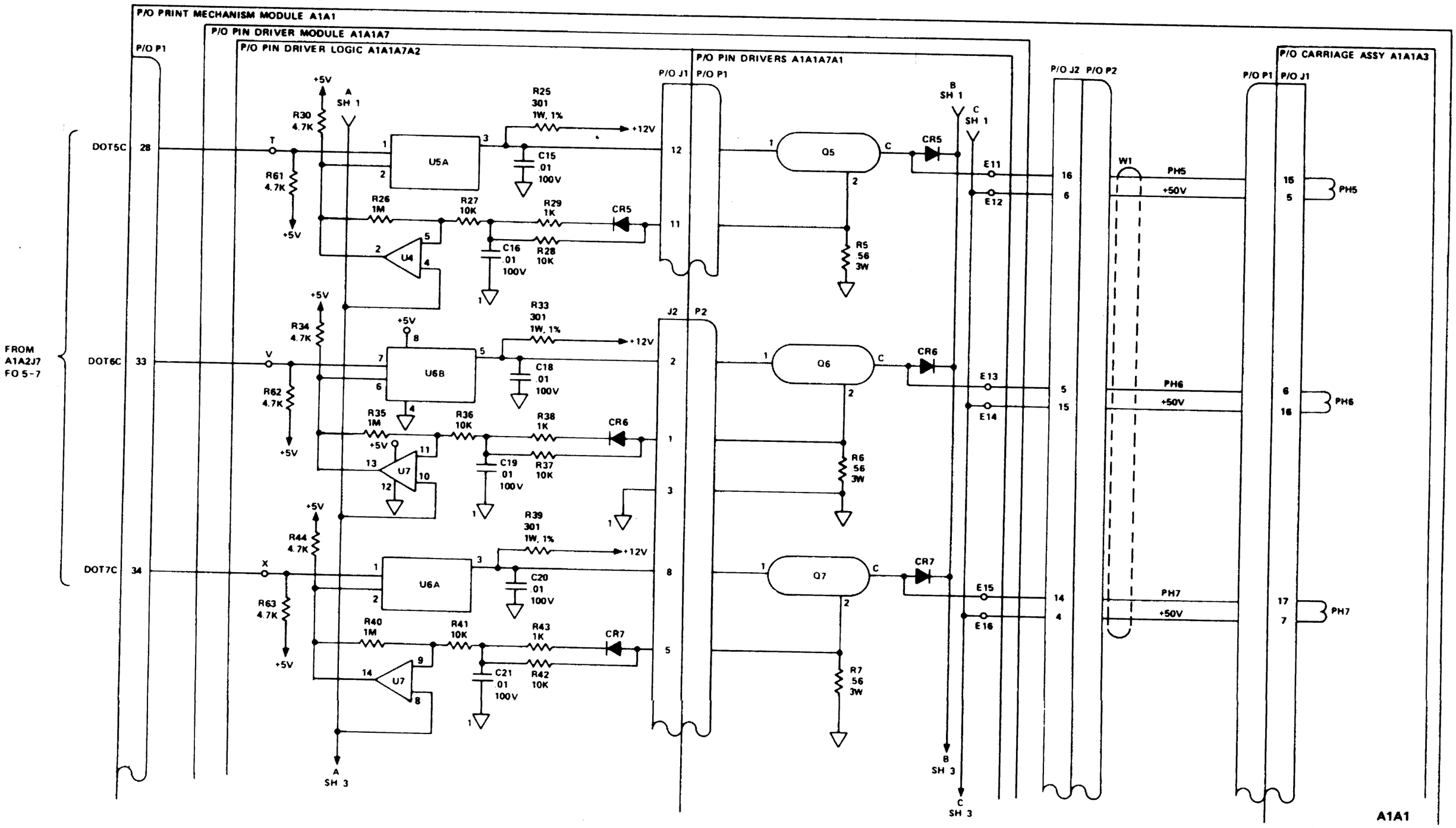


Figure FO 5-8. Print Mechanism (A1A1), Schematic Diagram (Sheet 2 of 7)

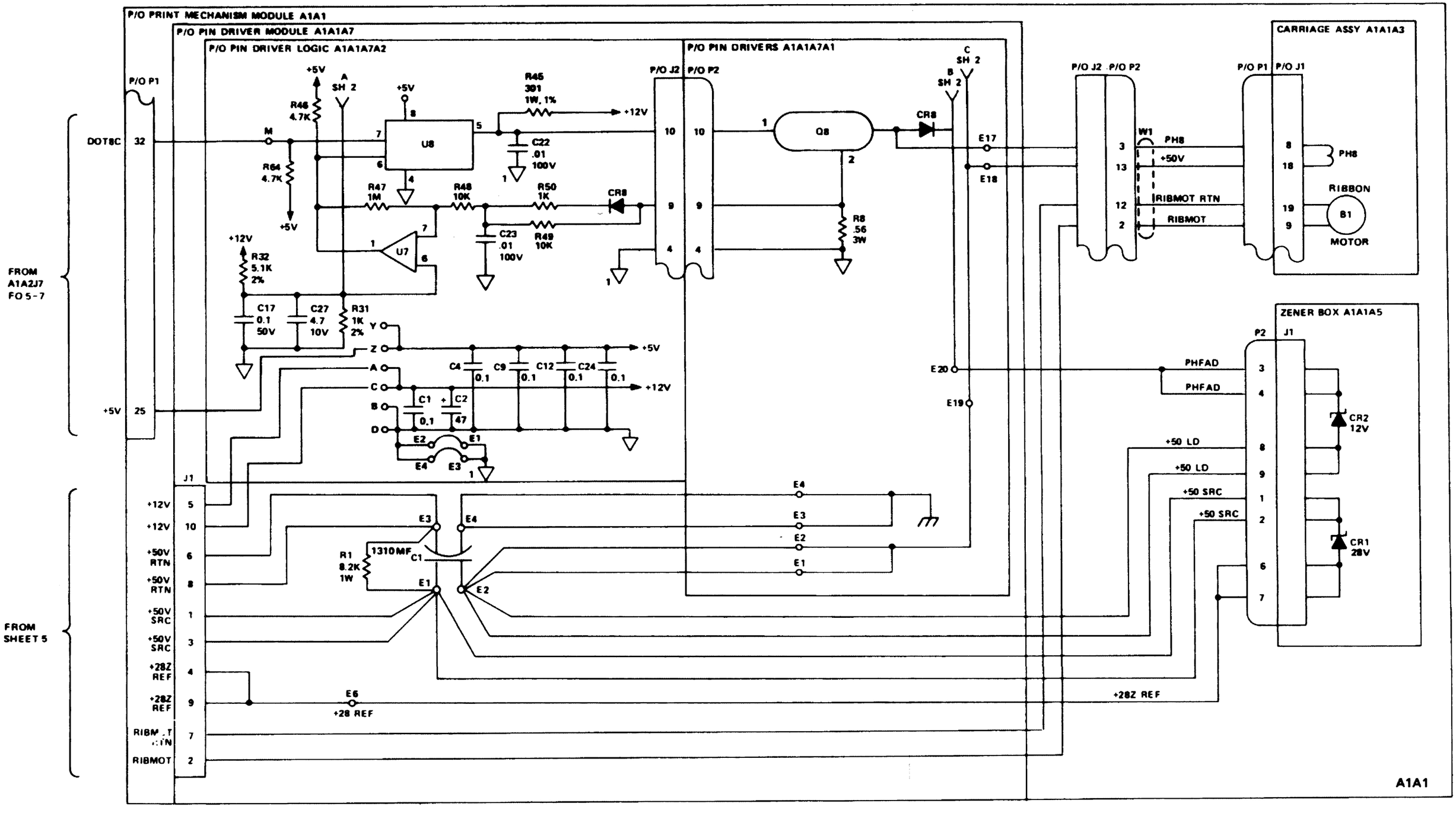


Figure FO 5-8. Print Mechanism (A1A1), Schematic Diagram (Sheet 3 of 7)

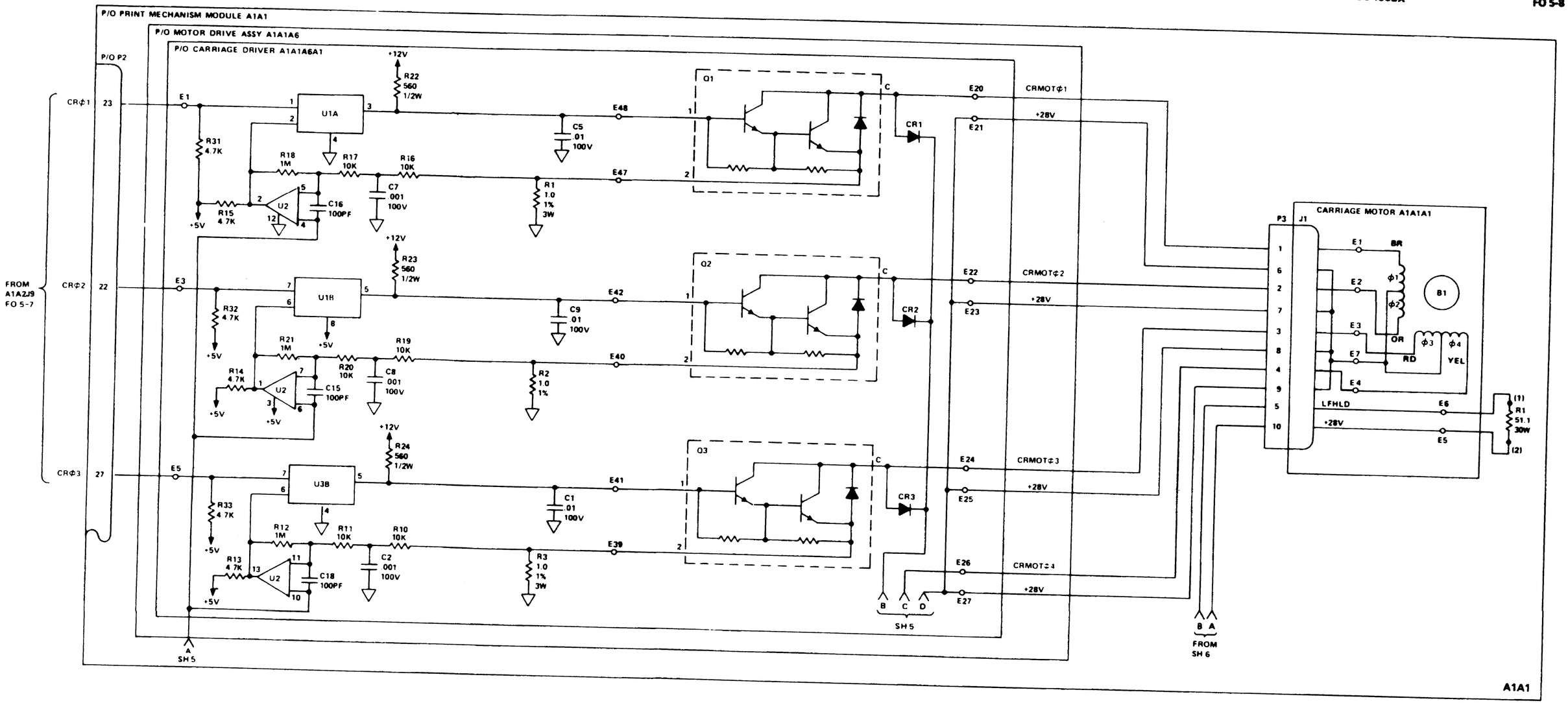


Figure FO 5-8. Print Mechanism (A1A1), Schematic Diagram (Sheet 4 of 7)

Original

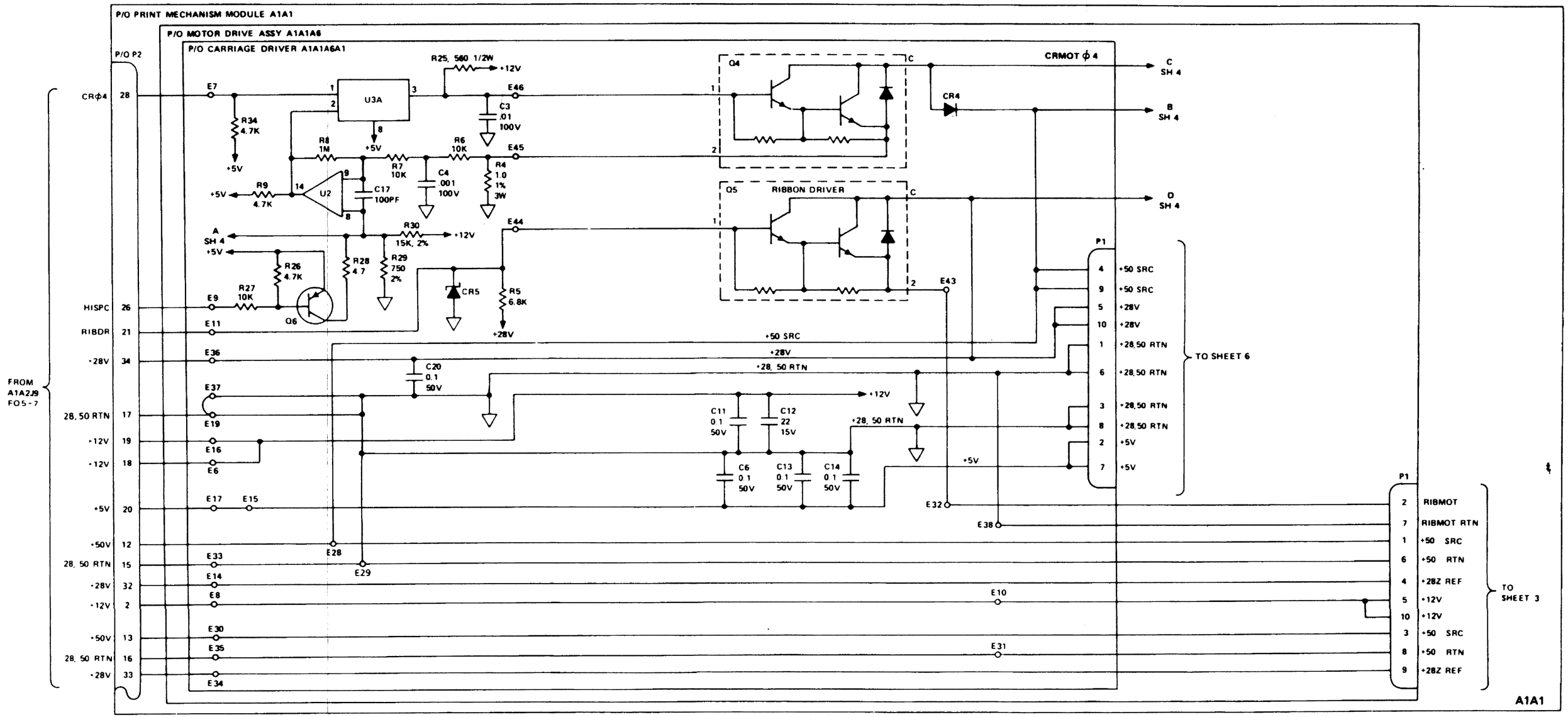


Figure FO 5-8. Print Mechanism (A1A1), Schematic Diagram (Sheet 5 of 7)

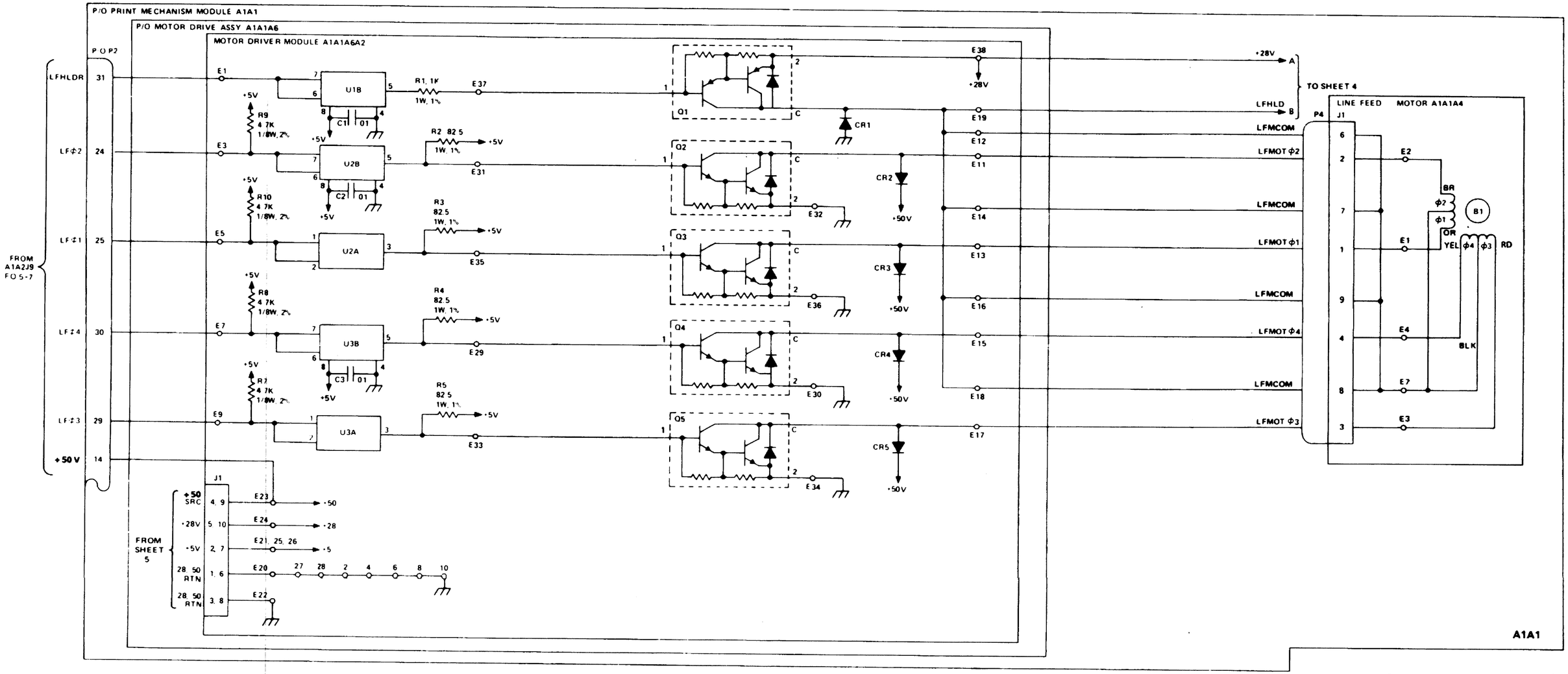


Figure FO 5-8. Print Mechanism (A1A1), Schematic Diagram (Sheet 6 of 7)

SPECIFIC NOTES

1. VALUES OF A1A1R1 AND A1A2R2 ARE SELECTED AT TEST.
2. VALUE OF A2R1 IS SELECTED AT TEST.

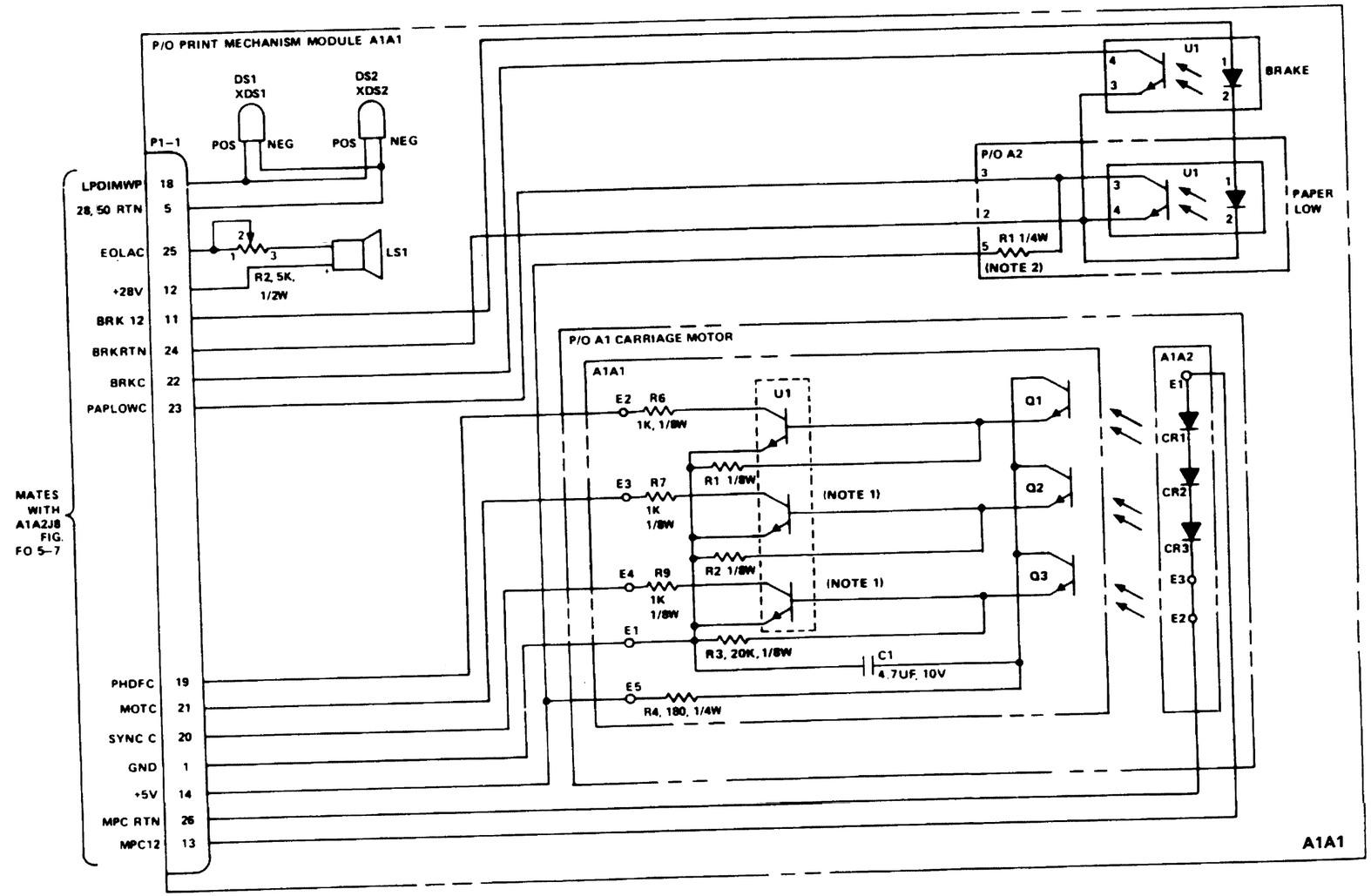


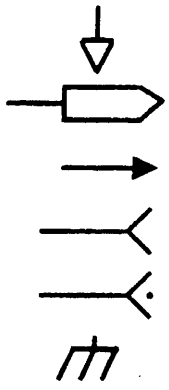
Figure FO 5-8. Print Mechanism (A1A1), Schematic Diagram (Sheet 7 of 7)

GENERAL NOTES

A. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS, 1/4 WATT.
CAPACITANCE VALUES ARE IN MICROFARADS.
INDUCTANCE VALUES ARE IN MICROHENRIES.

B. FOR POWER SUPPLY TO/FROM INFORMATION, REFER TO FIGURE FO 5-6 KEYBOARD PRINTER POWER DISTRIBUTION DIAGRAM.

C. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:



CIRCUIT GROUND

PULLUP

TO

FROM

TEST POINT

CHASSIS GROUND

D. COMPONENTS PHYSICALLY LOCATED ON HEAT SINK ASSEMBLY, BUT SHOWN FUNCTIONALLY AS PART OF THE POWER SUPPLY A2 SUBASEMBLY ARE AS FOLLOWS:

C1	CR14	L1	Q1	R4	T1	U1
C2	CR15	L2	Q2	R10	T2	U2
C7		L3	Q3	R11	T3	U3
C21		L4		R12	T4	U4
		L5				
		L6				
		L7				

REFERENCE DESIGNATIONS SHOULD BE PREFIXED WITH A1A3A1.

Figure FO 5-9. Power Supply A1A3, Schematic Diagram (Sheet 1 of 4)

SPECIFIC NOTES

1. THE FOLLOWING TABLE PROVIDES PRIMARY AND SECONDARY VOLTAGE AND CURRENT LEVELS FOR THE POWER TRANSFORMERS.

PARTS LOCATION INDEX

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
A3A1A1-C3	10B	A3A1A1-CR17	4C	A3A1A1-R25	11B	A3A1A1-R83	3C
-C21	4D	-CR18	4B	-R26	11B	-R84	4B
-C22	4C	-CR19	3B	-R27	10B	-R85	3B
-C23	3C	-CR20	3B	-R28	10B	-R86	4B
-C24	4B			-R29	10B	-R87	4B
-C28	11B	-Q8	11A	-R30	10B	-R88	4C
		-Q12	4D			-R89	3C
-CR5	9B	-Q13	4B	-R76	5D	-R90	3C
-CR6	9A	-Q14	3B	-R77	4D	-R91	3B
-CR7	10A	-R3	4D	-R78	5D	-R92	3B
-CR13	4D	-R21	9B	-R79	4D	-R93	10B
-CR14	4C	-R22	9A	-R80	4D	-R94	3C
-CR15	5B	-R23	9B	-R81	4D	-U2B	10B
-CR16	4B	-R24	11A	-R82	3C	-U4D	10B

Figure FO 5-9 Power Supply A1A3, Schematic Diagram (Sheet 2 of 4)

PARTS LOCATION INDEX - CONTINUED

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
A3A1[illegible]-U6	4C	A3A1A2-E3	3D	A3A1A2-E49	7C	A3A1A2-E99	10D
		-E4	2D	-E50	6C	-E100	10D
A3A1[illegible]-C1	10E	-E5	7D	-E51	6C	-E103	8D
-C2	11D	-E6	11D	-E52	9E	-E104	8D
-C3	9D	-E7	11D	-E53	9E	-E105	8E
-C4	9C	-E8	11D	-E54	9D	-E106	11E
-C5	8E	-E9	11D	-E55	9C	-E107	11D
-C6	8C	-E10	11D	-E56	8D	-E108	11E
-C7	8D	-E11	11D	-E57	10D	-E109	11E
-C8	7E	-E12	11D	-E58	8D		
-C9	7D	-E13	11D	-E59	10D	-L1	10E
-C10	7E	-E14	11D	-E60	8D	-L2	7E
-C11	6E	-E15	7D	-E61	10E	-L3	7D
-C12	6E	-E16	7D	-E63	9D	-L4	7D
-C13	6E	-E17	3E	-E64	9D	-L5	7B
-C14	3E	-E18	3E	-E65	9C		
-C15	3E	-E19	2E	-E66	9C	-Q1	9E
-C16	2E	-E20	7E	-E70	9E	-Q2	9D
-C17	2D	-E21	6E	-E71	9C	-Q3	6C
-C18	2C	-E22	6E	-E72	9C		
-C19	7C	-E23	7D	-E73	8D	-R1	11E
-C20	2B	-E24	7E	-E74	8D	-R2	9E
-C21	3A	-E25	3E	-E75	7C	-R3	9D
-C22	3A	-E26	7E	-E76	3B	-R4	8E
-C23	7B	-E27	3E	-E78	4A	-R6	6C
-C24	7A	-E28	6E	-E79	4A	-R7	7B
-C29	11E	-E29	6E	-E80	9D	-R8	7A
-C30	11E	-E30	6E	-E81	9D	-R9	4A
		-E31	11D	-E82	8C	-R11	10D
-CR2	11D	-E32	11D	-E83	11E	-R12	10E
-CR3	11D	-E33	7A	-E84	4A	-R13	3E
-CR4	9E	-E34	7B	-E85	3A		
-CR5	9C	-E35	8D	-E86	11E	-RT1	10D
-CR6	8A	-E36	8D	-E87	11C	-RT2	11C
-CR7	8D	-E37	8E	-E88	11C	-RT3	10D
-CR8	8E	-E38	7D	-E89	8D		
-CR9	7E	-E39	7D	-E90	8C	-T1	11D
-CR10	8D	-E40	7E	-E91	7C	-T2	9E
-CR11	7D	-E41	8E	-E92	8C	-T3	8D
-CR12	8C	-E42	7D	-E93	7C	-T4	8E
-CR13	7C	-E43	7A	-E94	7C		
-CR14	8B	-E44	7A	-E95	9E	-U1	6E
-CR15	7B	-E45	7B	-E96	9E	-U2	3E
		-E46	7B	-E97	7D	-U3	10E
-E1	7D	-E47	6C	-E98	10D	-U4	7B
-E2	3D						

WARNING

DANGEROUS VOLTAGES EXIST WHEN POWER IS ON.

* 61-40369 A1 ASSY

REF DES	-001	-002
C21	10µf, 20 V DC	22µf, 15 V DC
R94	-	1K, 1/4 WATT

** 61-40370 A2 ASSY

REF DES	-001, -002	-003, -004
R13	470Ω, 1/4 WATT	46.4Ω, 1 WATT

WARNING

DANGEROUS VOLTAGES EXIST WHEN POWER IS ON.

* 61-40369 A1 ASSY

REF DES	-001	-002
C21	10µf, 20 V DC	22µf, 15 V DC
R94	-	1K, 1/4 WATT

** 61-40370 A2 ASSY

REF DES	-001, -002	-003, -004
R13	470Ω, 1/4 WATT	46.4Ω, 1 WATT

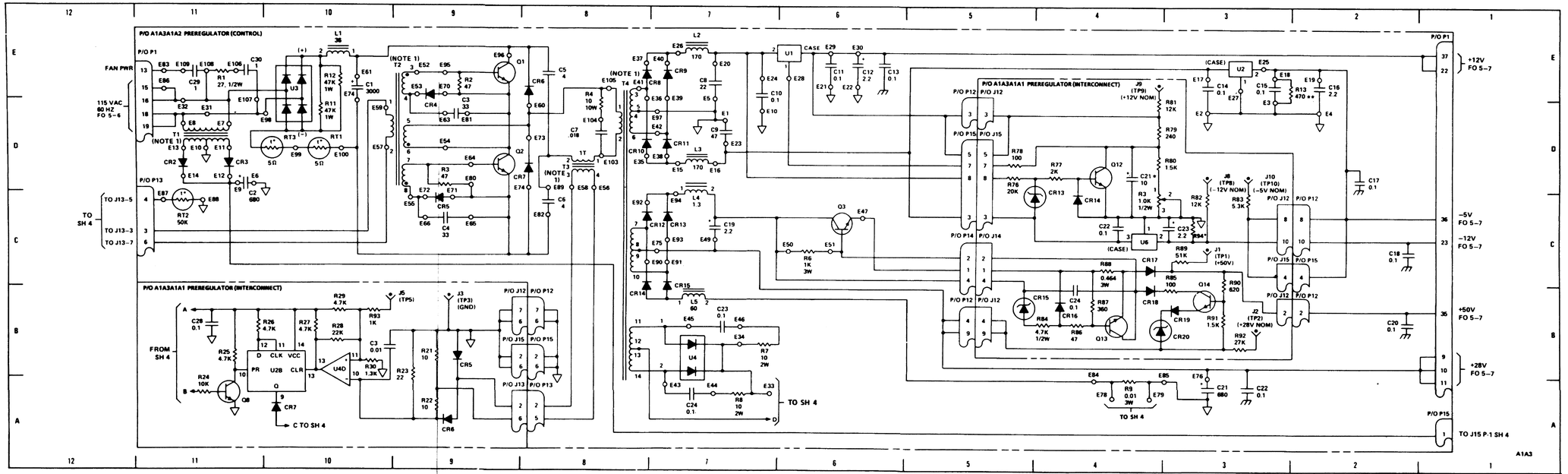


Figure 5-9. Power Supply (A1A3), Schematic Diagram (Sheet 3 of 4)

SPECIFIC NOTE

1. PREFERRED VALUE FOR R57 IS 3K; ALTERNATE VALUES OF 2.7K AND 2.4K MAY BE USED TO ACHIEVE 50-62 KHZ OPERATING FREQUENCY.

PARTS LOCATION INDEX

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
A3A1A1-C1	11C	A3A1A1-Q3	8E	A3A1A1-R38	10B	A3A1A1-R73	6B
-C2	7D	-Q4	8E	-R39	10B	-R74	5C
-C4	8C	-Q5	9D	-R40	9A	-R75	5C
-C5	7C	-Q6	7D	-R41	10A		
-C6	10D	-Q7	9C	-R42	10A	-U1	10D
-C7	10D	-Q9	6D	-R43	8B	-U2A	9D
-C8	9D	-Q10	8B	-R44	8C	-U3	8C
-C9	9B	-Q11	6B	-R45	8B	-U4A	9B
-C10	9B			-R46	8B	-U4B	9C
-C11	9A	-R1	10D	-R47	7B	-U4C	9A
-C12	7B	-R2	7B	-R48	7B	-U5A	7A
-C13	7A	-R4	9E	-R49	8B	-U5B	6B
-C14	6D	-R5	10E	-R50	8A	-U5C	6D
-C15	4D	-R6	10D	-R51	8A	-U5D	8B
-C16	5D	-R7	10D	-R52	7B		
-C17	6C	-R8	11D	-R53	7A	A3A1A2-C25	3D
-C18	5C	-R9	10C	-R54	7B	-C26	2D
-C19	5C	-R10	9D	-R55	7B	-C27	1E
-C20	6C	-R11	9D	-R56	7B	-C28	1D
-C25	10B	-R12	8D	-R57	8C		
-C26	9A	-R13	8D	-R58	7C	-E48	3E
-C27	9C	-R14	9D	-R59	6D	-E62	2D
		-R15	9E	-R60	6D	-E67	2D
-CR1	10D	-R16	8D	-R61	6D	-E68	2D
-CR2	10C	-R17	8D	-R62	6D	-E69	2E
-CR3	9E	-R18	7D	-R63	5D	-E77	2D
-CR4	7E	-R19	7D	-R64	6D	-E101	2E
-CR8	10B	-R20	7D	-R65	4D	-E102	3E
-CR9	10A	-R31	10D	-R66	6D		
-CR10	8A	-R32	10D	-R67	6C	-L6	3E
-CR11	5D	-R33	9D	-R68	6C	-L7	3E
-CR12	6D	-R34	9D	-R69	6C		
		-R35	10C	-R70	6B	-R5	1D
-Q1	10E	-R36	10B	-R71	6C	-R10	2D
-Q2	10D	-R37	10B	-R72	6C		

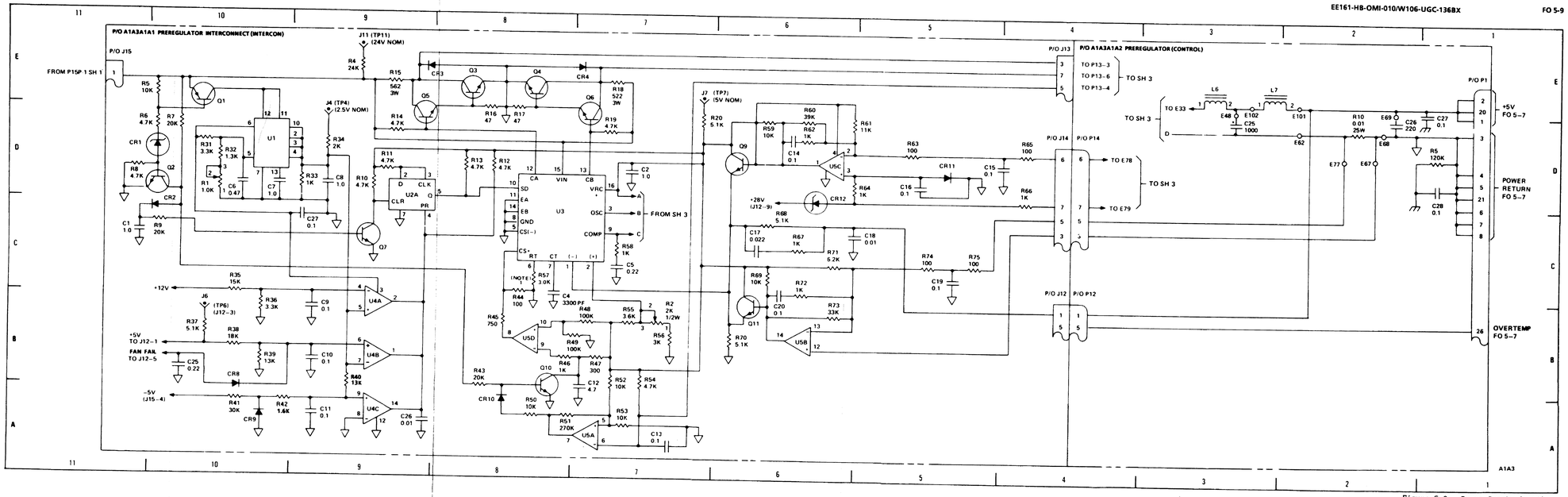


Figure 5-9. Power Supply (A1A3), Schematic Diagram (Sheet 4 of 4)

1. THE ADDRESS BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS. THE FOLLOWING IS THE ROUTING LIST (REFER TO FO 5-11).

ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE
AB00	J2-A28	AB06	J2-B29	AB11	J2-B28
AB01	J2-A27	AB07	J2-B30	AB12	J2-A32
AB02	J2-A29	AB08	J2-B31	AB13	J2-A26
AB03	J2-B26	AB09	J2-B32	AB14	J2-A25
AB04	J2-A30	AB10	J2-B27	AB15	J2-B25
AB05	J2-A31				

2. THE SYSTEM DATA BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS. THE FOLLOWING IS A LIST OF THE SOURCE FOR EACH BIT:

SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE
SDB0	J2-A9	SDB3	J2-B9	SDB6	J2-A6
SDB1	J2-A8	SDB4	J2-B7	SDB7	J2-B6
SDB2	J2-A7	SDB5	J2-B8		

PARTS LIST INDEX

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
A1A5C1	15C	A1A5E2	1A	A1A5R24	5A	A1A5U48A	14A
C2	12D	E3	2A	R25	4A	U49B	7B
C3	11D	E4	2A	R26	5A	U49C	9B
C4	10D	E5	1A			U49D	12A
C5	15D	E6	2A			U50A	4B
C6	9D			U1	15B	U50B	1A
C7	8D	J1	13A	U2	12C	U50C	15A
C9	5D	J2	11A	U3	11C	U50E	15A
C10	4D	J3	2D	U4	10C	U50F	14A
C11	16D	J4	12A	U5	15C	U50G	16A
C25	3D	J5	10B	U6	9C	U51C	7B
C26	16C	J6	8B	U7	8C	U51D	7B
C39	16B	J7	8B	U9	5C	U52B	7B
C40	11A	J8	2D	U10	4C	U52C	7B
C41	14B			U11	16D	U53	2A
C42	16A	R1	10B	U27	16C	U54A	2B
C43	16A	R2	8B	U44	16B	U54B	2C
C44	7B	R3	8B	U45A	13B	U55B	3E
C45	6B	R4	2D	U45B	10B	U55C	3B
C46	2B	R13	16A	U45C	6A	U55D	3B
C47	2B	R15	6B	U45D	15B	U56A	4B
C48	3C	R16	2D	U46A	11B	U56B	5B
C49	5B	R18	6B	U46B	12B	U57A	3A
C50	13A	R19	11A	U46C	11A	U57B	13A
C51	4A	R20	11A	U46D	11B	U57C	5A
C53	2D	R21	2D	U47A	9B	U57D	4A
		R22	2D	U47B	9A		
E1	2B	R23	4A	U47C	15A	Y1	4A

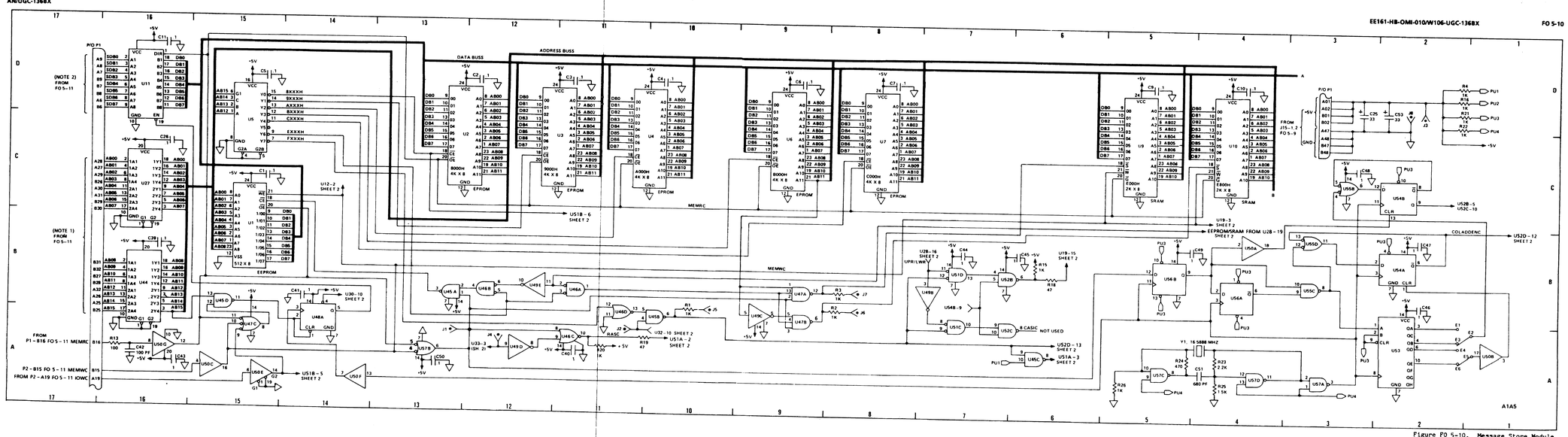


Figure FO 5-10. Message Store Module (A1A5), Schematic Diagram (Sheet 1 of 2)

Original

PARTS LIST INDEX

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
A1A5C28	8A	A1A5U13	16C	A1A5U28	9B
C29	14A	U14	16B	U29	8B
C30	4A	U15	14B	U30	6B
		U16	14B	U31	14B
R5	2C	U17	4C	U32	14A
R6	2B	U18	3C	U33	2C
R7	2B	U19	11D	U34	4B
R8	2C	U20	10D	U35	3B
R9	2B	U21	9D	U49A	10B
R10	2B	U22	9D	U49F	16C
R11	2A	U23	8D	U51A	17C
R12	2A	U24	7D	U51B	10B
		U25	7D	U52A	17B
U12	11A	U26	5D	U52D	17B

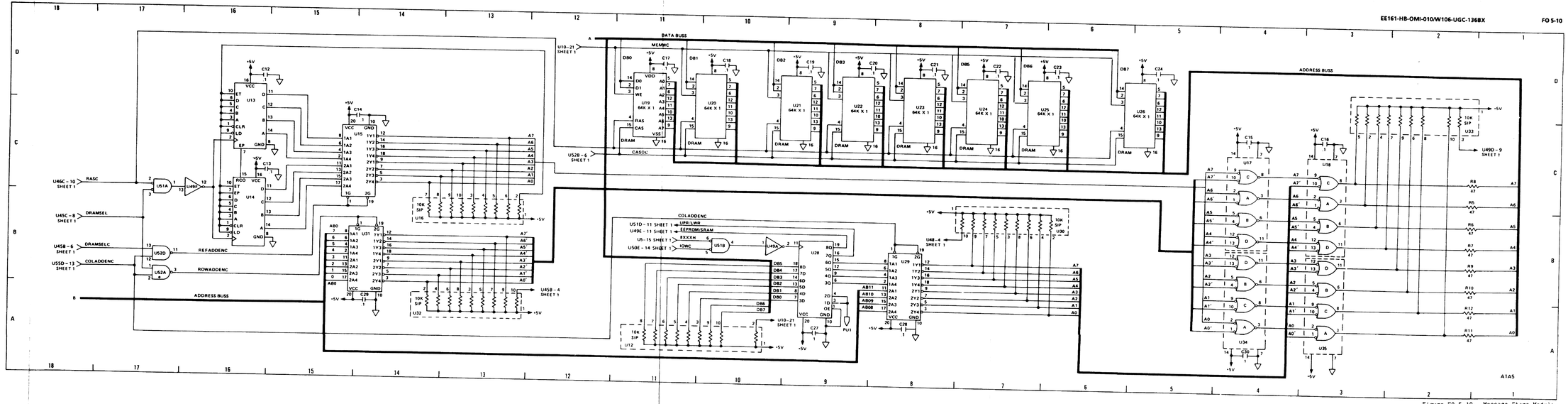
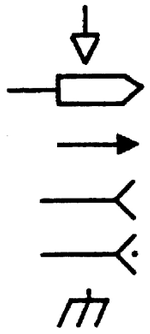


Figure FO 5-10. Message Store Module (A1A5), Schematic Diagram (Sheet 2 of 2)

GENERAL NOTES

A. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS, 1/8 WATT.
CAPACITANCE VALUES ARE IN MICROFARADS.
INDUCTANCE VALUES ARE IN MICROHENRIES.

B. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:



CIRCUIT GROUND

PULLUP

TO

FROM

TEST POINT

CHASSIS GROUND

SPECIFIC NOTES

1. THE ADDRESS BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS (i.e., AB10 J2-B27, J1-B27, J3-B27, AND J4-B27). THE FOLLOWING IS THE ROUTING LIST:

ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE
AB00	A28	AB06	B29	AB11	B28
AB01	A27	AB07	B30	AB12	A32
AB02	A29	AB08	B31	AB13	A26
AB03	B26	AB09	B32	AB14	A25
AB04	A30	AB10	B27	AB15	B25
AB05	A31				

2. THE SYSTEM DATA BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS. THE FOLLOWING IS THE ROUTING LIST:

SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE
SDB0	A9	SDB3	B9	SDB6	A6
SDB1	A8	SDB4	B7	SDB7	B6
SDB2	A7	SDB5	B8		

3. CAPACITOR "C3" TO BE SELECTED AT TEST FROM THE FOLLOWING VALUES: 1 PF, 5 PF THRU 8 PF, 10 PF, 12 PF, 15 PF, 18 PF, 22 PF, 27 PF, AND 33 PF.

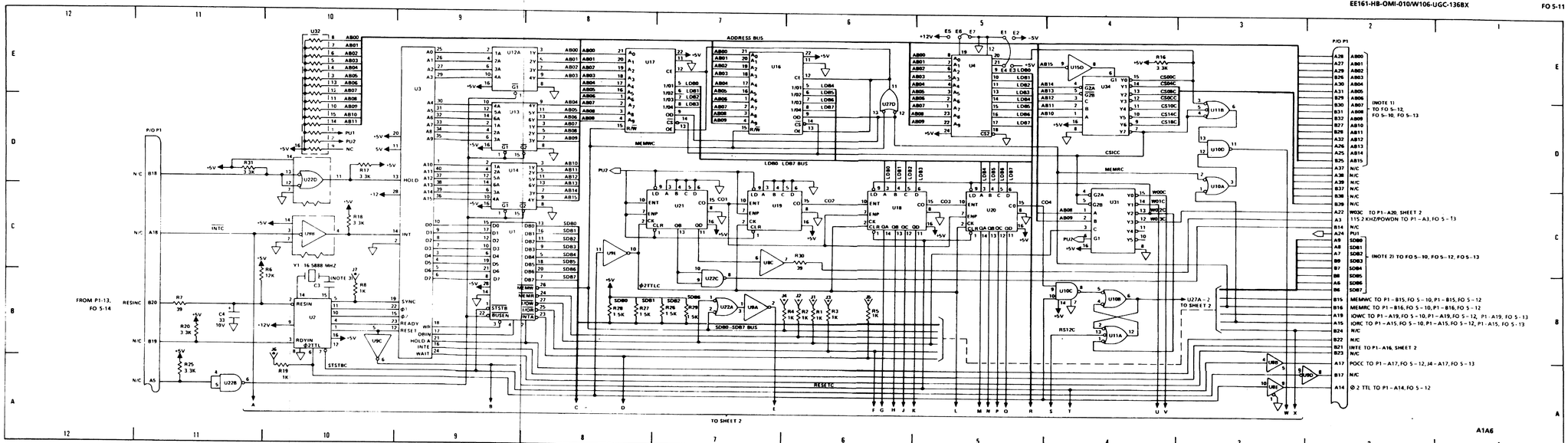
PARTS LIST INDEX

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
C3	10B	R2	6B	U1	9C	U13	9D
C4	11B	R3	6B	U2	10B	U14	9D
		R4	6B	U3	9E	U15D	4E
		R5	6B	U4	5E	U16	7E
E1	5E	R6	10B	U8B	3B	U17	8E
E2	5E	R7	11B	U8C	7C	U18	6C
E3	5E	R8	10B	U8E	3A	U19	7C
E4	5E	R16	4E	U9A	7B	U20	5C
E5	5E	R17	10D	U9B	10C	U21	7C
E6	5E	R18	10C	U9C	10B	U22A	7B
E7	5E	R19	10A	U9D	2A	U22B	11A
		R20	11B	U9E	8C	U22C	7B
J1	7B	R25	11A	U10A	3D	U22D	10D
J2	7B	R26	7B	U10B	4B	U27D	6D
J3	7B	R27	8B	U10C	4B	U31	4C
J4	6B	R28	8B	U10D	3D	U32	10E
J5	7B	R29	7B	U11A	4B	U34	4E
		R30	6C	U11B	3D		
R1	6B	R31	11D	U12A	9E	Y1	10B

FP 5-55

PARTS LIST INDEX

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
C3	10B	R2	6B	U1	9C	U13	9D
C4	11B	R3	6B	U2	10B	U14	9D
		R4	6B	U3	9E	U15D	4E
		R5	6B	U4	5E	U16	7E
E1	5E	R6	10B	U8B	3B	U17	8E
E2	5E	R7	11B	U8C	7C	U18	6C
E3	5E	R8	10B	U8E	3A	U19	7C
E4	5E	R16	4E	U9A	7B	U20	5C
E5	5E	R17	10D	U9B	10C	U21	7C
E6	5E	R18	10C	U9C	10B	U22A	7B
E7	5E	R19	10A	U9D	2A	U22B	11A
		R20	11B	U9E	8C	U22C	7B
J1	7B	R25	11A	U10A	3D	U22D	10D
J2	7B	R26	7B	U10B	4B	U27D	6D
J3	7B	R27	8B	U10C	4B	U31	4C
J4	6B	R28	8B	U10D	3D	U32	10E
J5	7B	R29	7B	U11A	4B	U34	4E
		R30	6C	U11B	3D		
R1	6B	R31	11D	U12A	9E	Y1	10B



Original

Figure FO 5-11. Microcomputer Module (A1A6), Schematic Diagram (Sheet 1 of 2)

PARTS LIST INDEX

REF DES	ZONE	REF DES	ZONE	REF DES	ZONE	REF DES	ZONE
		J8	6B	R33	9D	U11C	8C
C1	10B	J9	6B	R34	10D	U12B	8D
C2	9B	J10	6B	R35	10D	U15B	9C
C5	9B	J11	6B	R36	9D	U15C	9C
C6	9B	J12	7B	R37	9D	U15E	9C
C7	9B	J13	7B	R38	9D	U15F	9C
C8	9B			R39	9D	U23	5D
C9	9B	R9	6B	R40	9C	U24	4D
C10	8B	R10	6B	R41	9C	U25	3D
C11	10B	R11	6B	R42	10C	U26	3E
C12	9B	R12	6B	R43	10C	U27A	6A
C13	9B	R13	7B	R44	8B	U27B	8C
C14	9B	R14	7B			U28	6B
C15	10B	R15	4C			U29	7B
C16	10B	R21	9C	U5	7D	U30	4B
C17	9B	R22	9C	U6	6D	U33	3D
C18	9B	R23	10C	U7	6D	U35	5B
C19	8B	R24	9C	U8F	3E	U36	3B
C20	10C	R32	9D	U9F	4C	U37	4B

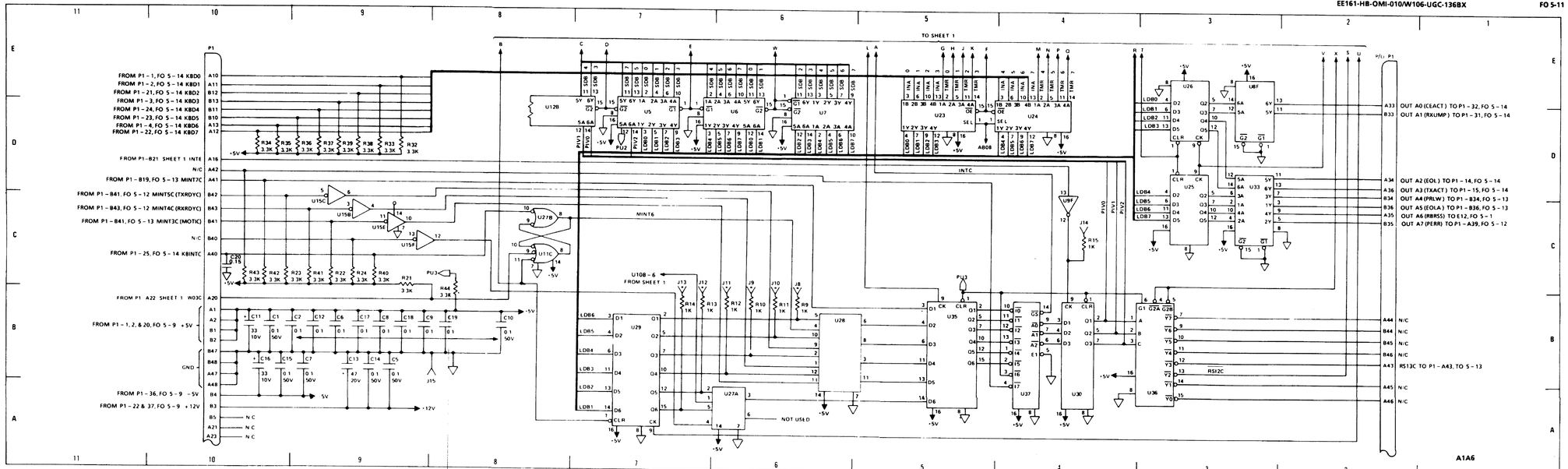


Figure FO 5-11. Microcomputer Module (A1A6), Schematic Diagram (Sheet 2 of 2)

Original

GENERAL NOTES

A. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS, 1/4 WATT.
CAPACITANCE ALUES ARE IN MICROFARADS.

B. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

CIRCUIT GROUND

PULLUP

TO

FROM

TEST POINT

CHASSIS GROUND

SPECIFIC NOTES

. THE ADDRESS BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS. THE FOLLOWING IS THE ROUTING LIST (REFER TO FO 5-11):

ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE
AB00	J2-A28	AB06	J2-B29	AB11	J2-B28
AB01	J2-A27	AB07	J2-B30	AB12	J2-A32
AB02	J2-A29	AB08	J2-B31	AB13	J2-A26
AB03	J2-B26	AB09	J2-B32	AB14	J2-A25
AB04	J2-A30	AB10	J2-B27	AB15	J2-B25
AB05	J2-A31				

PARTS LOCATION INDEX

A1A7C1	7D	A1A7J11	1D
C2	5D		
C3	4D	P1	D10
C4	3D		
C13	8C	R11	2D
C15	9D	R12	2D
C15	9D	R13	2D
C16	9C		
		U1	7D
E1	7C	U2	5D
E2	7C	U3	4D
E3	7C	U4	3D
E4	5C	U11B	6A
E5	5C	U11C	7B
E6	5C	U12	8B
E7	5C	U14	9D
E8	4C	U15	9B
E9	4C	U24B	7B
		U31B	9A
J9	2D	U42A	9A
J10	2D		

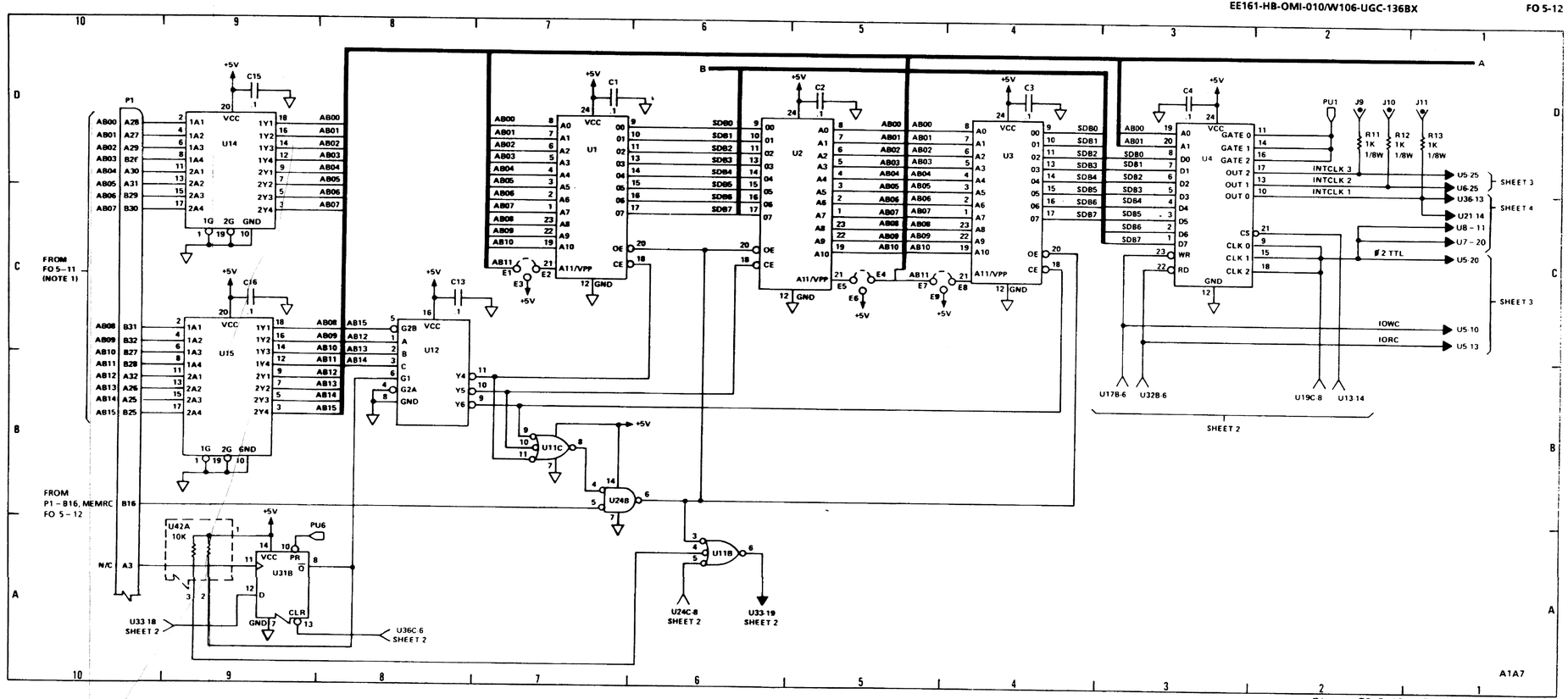


Figure FO 5-12. Interface Module (A1A7), Schematic Diagram (Sheet 1 of 4)

SPECIFIC NOTES

THE SYSTEM DATA BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS. THE FOLLOWING IS THE ROUTING LIST (REFER TO FO 5-11):

SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE
SDB0	J2-A9	SDB3	J2-B9	SDB6	J2-A6
SDB1	J2-A8	SDB4	J2-B7	SDB7	J2-B6
SDB2	J2-A7	SDB5	J2-B8		

PARTS LOCATION INDEX

A1A7C11	3D	A1A7U19C	13D
C14	10C	U20	4B
C17	2D	U21	2B
C18	13C	U22	3C
C19	11B	U23	2C
C20	12B	U24A	11C
C37	4D	U24C	10C
C38	4D	U24D	10C
C39	7B	U25A	11D
C41	6B	U25B	11D
C43	7B	U28	4C
C44	7A	U29A	6B
C47	6D	U29B	6A
		U30A	6D
E10	11C	U30B	6C
E11	11C	U31A	12D
E12	11C	U32A	9B
		U32B	13C
J7	1D	U32C	9C
J8	1C	U32D	9B
		U33	12C
P1	9A	U34	11A
	13D	U35	12B
		U36A	11C
R9	1D	U36B	13D
R10	1C	U36C	12D
R19	3B	U36D	13D
		U39	4C
		U42	11A
U13	11C	U43	13B
U17B	13D	U44	8D

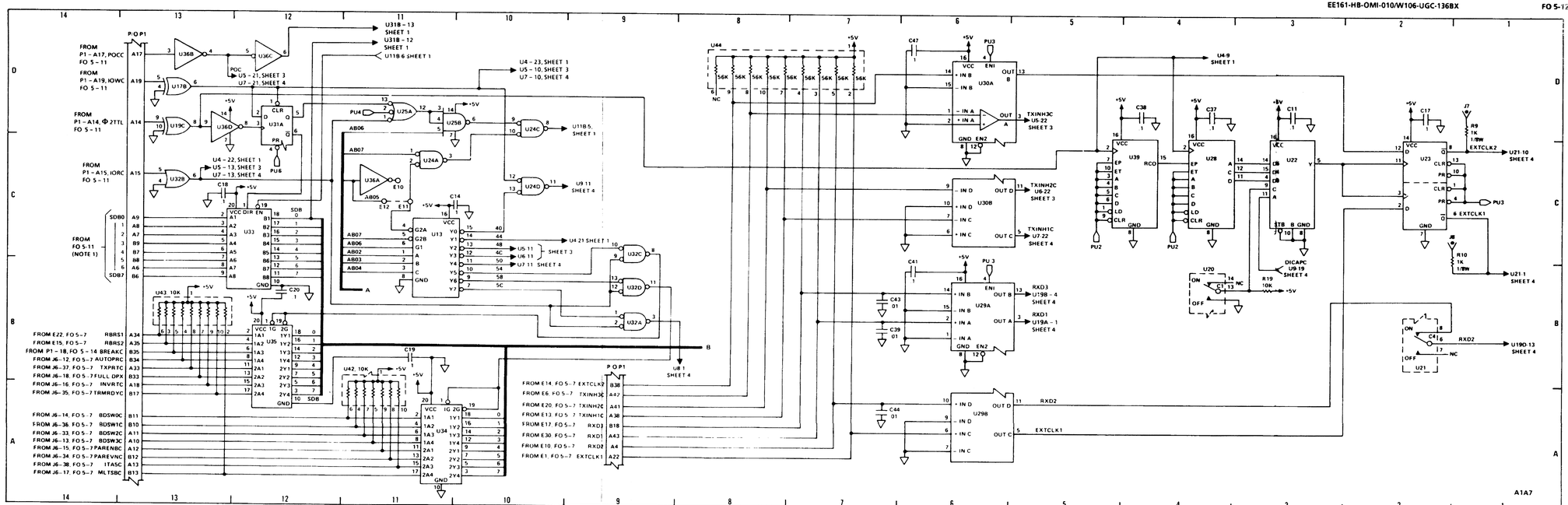


Figure FO 5-12. Interface Module (A1A7), Schematic Diagram (Sheet 2 of 4)

Original

PARTS LOCATION INDEX

A1A7C5	9D	A1A7P1	2C
C6	9B		
C21	5C	R7	6B
C22	5B	R8	6D
C23	3C		
C24	3C	U5	9D
C25	4C	U6	9B
C26	4C	U16A	7C
C27	3C	U16B	7B
C28	2D	U17A	6D
		U17C	6B
J5	6C	U26	5C
J6	6D	U38B	3D

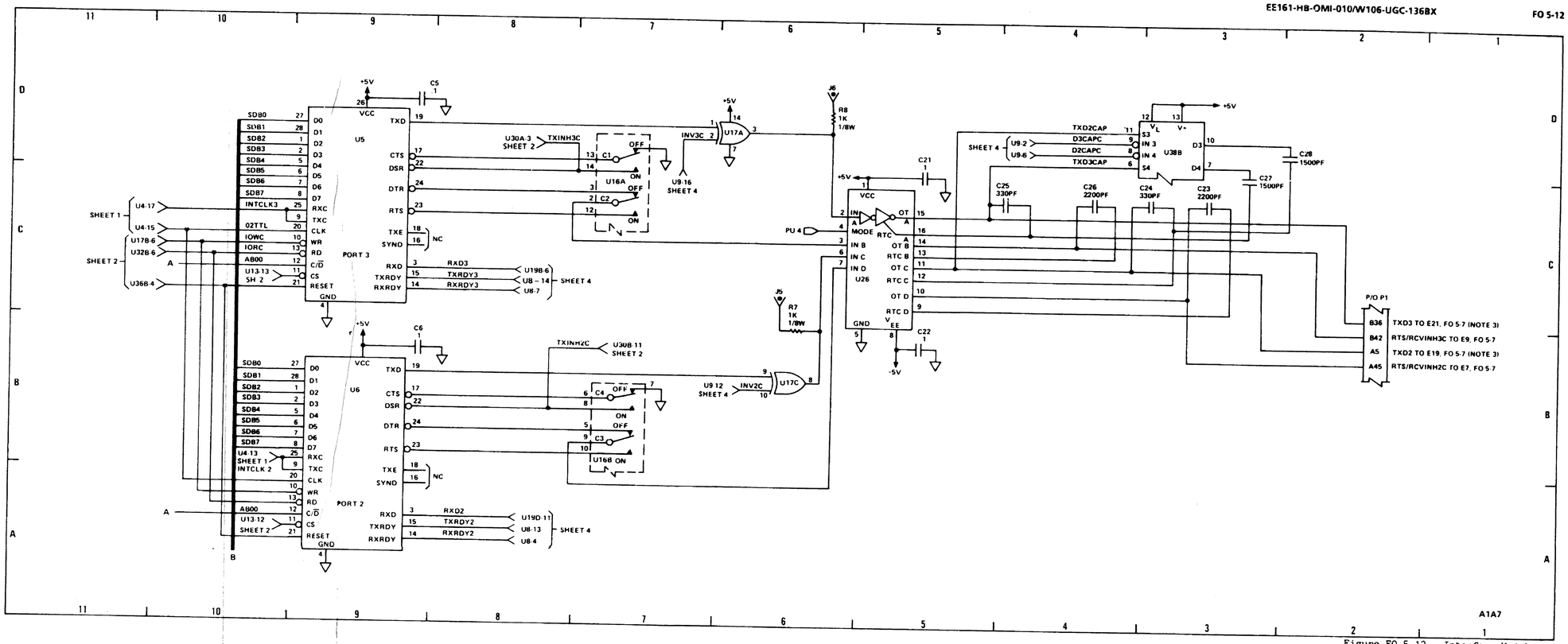


Figure FO 5-12. Interface Module (A1A7), Schematic Diagram (Sheet 3 of 4)

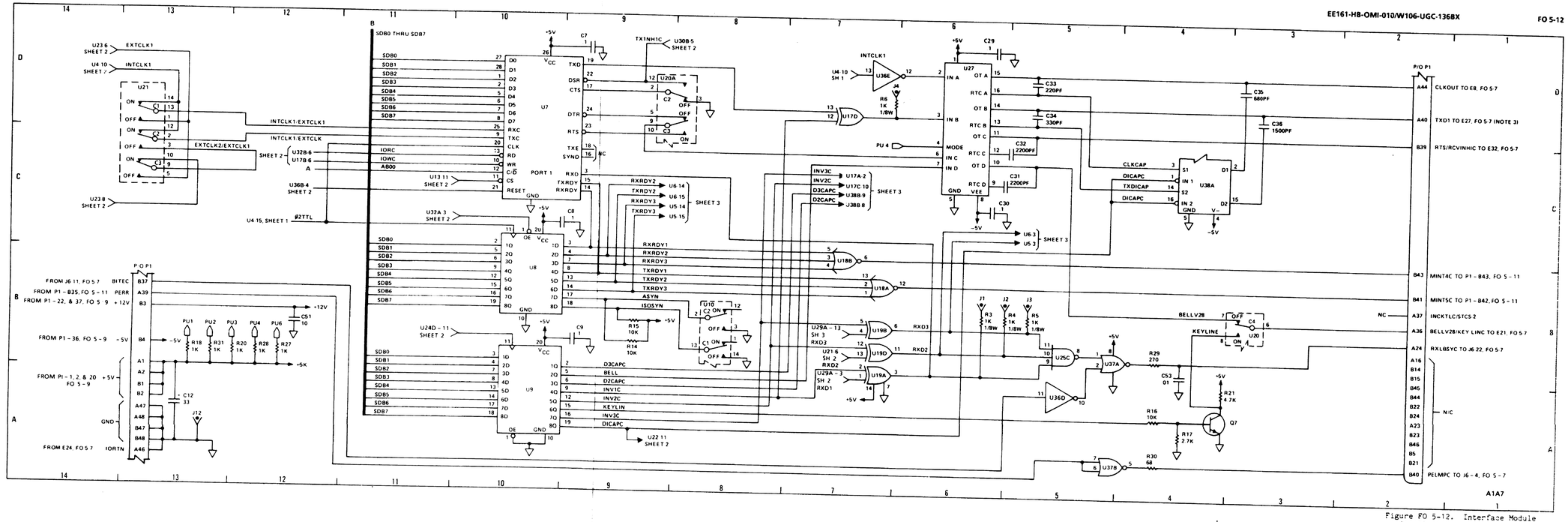
Original

SPECIFIC NOTES

1. THE TXD1 OUTPUT SIGNAL IS BIPOLAR +5 VDC TO -5 VDC.

PARTS LOCATION INDEX

A1A7C7	9D	A1A7R16	4A
C8	9C	R17	4A
C9	9B	R18	13B
C12	13A	R20	12B
C29	6D	R21	4A
C30	6C	R27	12B
C31	5C	R28	12B
C32	5C	R29	4B
C33	5D	R30	4A
C34	5D	R31	13B
C35	3D		
C36	3D	U7	10D
C51	12B	U8	10B
C53	4B	U9	10A
		U10	8B
J1	6B	U17D	7D
J2	6B	U18A	7B
J3	5B	U18B	7C
J4	7D	U19A	7B
J12	13A	U19B	7B
		U19D	7B
P1	13B, 2D	U20A	9D
		U20B	3B
Q7	4A	U21	13D
		U25C	5B
R3	6B	U27	6D
R4	6B	U36D	5A
R5	5B	U36E	7D
R6	7D	U37A	5B
R14	9B	U37B	5A
R15	9B	U38A	4C



Original

Figure FO 5-12. Interface Module (A1A7), Schematic Diagram (Sheet 4 of 4)

GENERAL NOTES

A. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS, 1/8 WATT.
CAPACITANCE VALUES ARE IN MICROFARADS.

B. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

CIRCUIT GROUND

PULLUP

TO

FROM

TEST POINT

CHASSIS GROUND

PARTS LOCATION INDEX

A1A8C1	8A	A1A8P1	11D, 4A	A1A8R38	10C	A1A8U1A	8A
C3	9A			R39	10C	U1B	8A
C8	2A			R40	11C	U1C	9A
C17	11B	Q1	7A	R41	11B	U1D	10A
C18	10A			R42	10B	U2A	5D
C22	2A	R1	9A	R43	10B	U2B	5C
C24	1A	R2	9A	R44	11C	U3A	6C
C26	11D	R3	8A	R45	10C	U3B	3B
C28	11C	R4	7A	R46	10C	U3D	3C
C29	11C	R5	7A	R47	10B	U4A	3C
C30	11B	R6	3A	R48	10C	U4B	3B
C33	1A	R7	4C	R49	10C	U5D	6D
C34	1A	R9	5C	R50	10A	U7A	6C
		R10	9B	R51	10B	U7B	6C
		R11	5B	R52	10B	U9C	6C
		R12	3C	R53	11B	U11	7C
J3	4C	R13	8B	R59	2A	U21A	10D
J5	6C	R16	4B	R60	6A	U21D	10C
J6	9B	R17	6D	R61	5B	U22A	10C
J7	5B	R19	9C	R62	6B	U22B	10B
J8	3C	R24	6B	R63	5B	U22C	10B
J9	8B	R29	5D	R64	5A	U22D	5A
J12	4B	R31	3A	R65	5A	U23	9B
J13	6D	R33	9D	R68	11A	U24	10D
J15	9C	R34	10D	R69	10B	U25	9C
J21	5D	R35	11D	R74	2A	U33B	9D
J23	6B	R36	10D	R76	9A		
J27	2A	R37	10C	R77	10A	Y1	9A

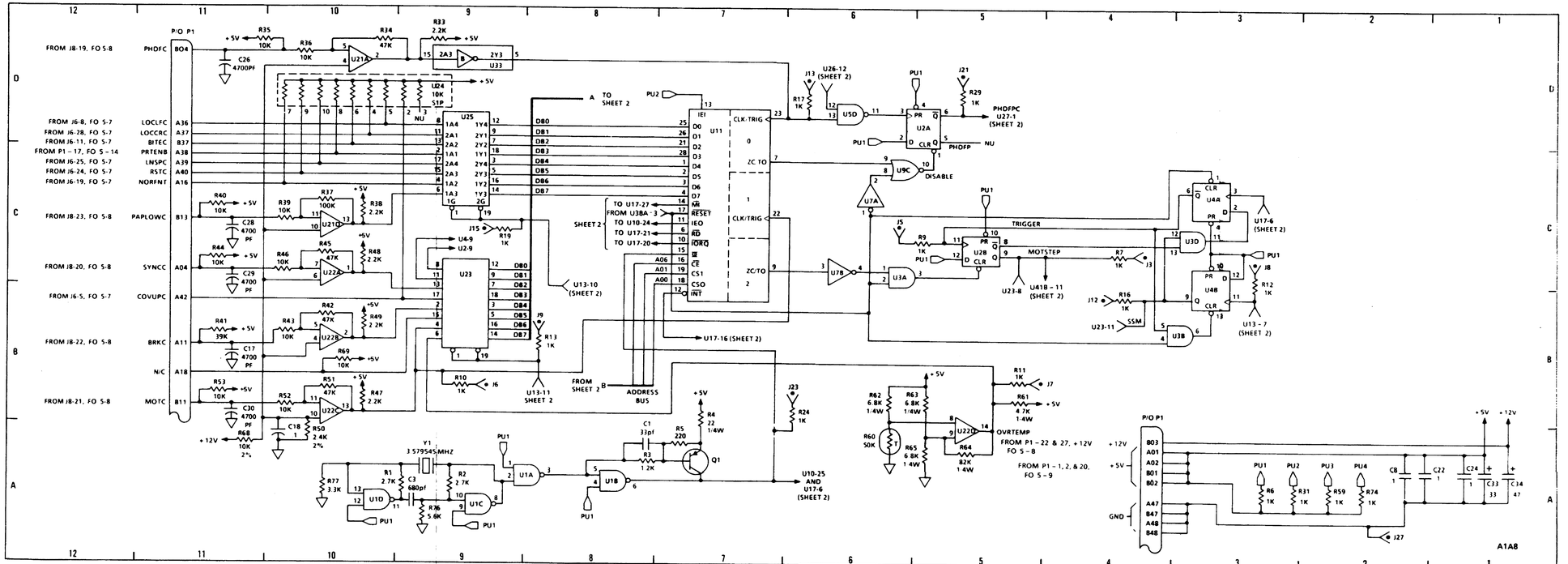


Figure FO 5-13. Controller Module A1A8, Schematic Diagram (Sheet 1 of 2)

Original

SPECIFIC NOTES

1. THE ADDRESS BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS. THE FOLLOWING IS THE ROUTING LIST (REFER TO FO 5-11).

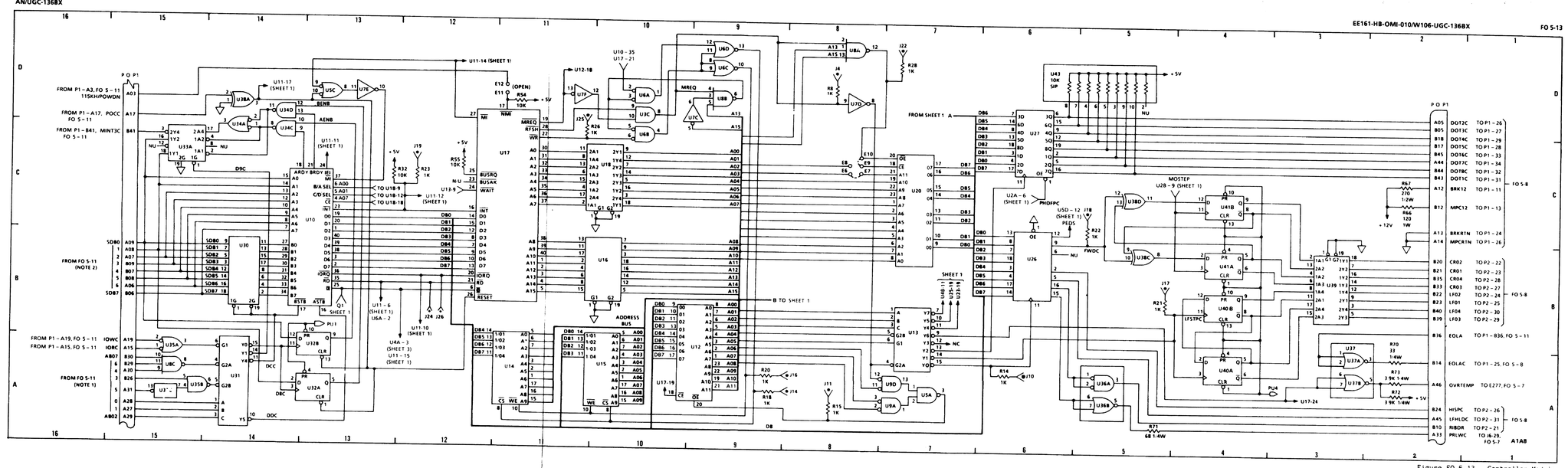
ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE	ADDRESS BIT	SOURCE
AB00	J2-A28	AB06	J2-B29	AB11	J2-B28
AB01	J2-A27	AB07	J2-B30	AB12	J2-A32
AB02	J2-A29	AB08	J2-B31	AB13	J2-A26
AB03	J2-B26	AB09	J2-B32	AB14	J2-A25
AB04	J2-A30	AB10	J2-B27	AB15	J2-B25
AB05	J2-A31				

2. THE SYSTEM DATA BUS IS ROUTED TO ALL FOUR LOGIC MODULES USING THE SAME PIN NUMBERS FOR ALL FOUR JACKS. THE FOLLOWING IS A LIST OF THE SOURCE FOR EACH BIT:

SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE	SYSTEM DATA BIT	SOURCE
SDB0	J2-A9	SDB3	J2-B9	SDB6	J2-A6
SDB1	J2-A8	SDB4	J2-B7	SDB7	J2-B6
SDB2	J2-A7	SDB5	J2-B8		

PARTS LOCATION INDEX

A1A8E11	11D	A1A8R18	9A	A1A8U7C	9D
E12	12D	R20	9A	U7D	8D
		R21	9B	U7E	13D
J4	8D	R23	12C	U7F	11D
J10	6A	R26	11D	U8A	8D
J11	8A	R28	7D	U8B	9D
J14	8A	R32	13C	U8C	15A
J16	8A	R54	11D	U9A	7A
J17	5B	R55	12C	U9D	7A
J18	5C	R66	2C	U10	13C
J19	12C	R67	2C	U12	9A
J22	7D	R70	2A	U13	7B
J24	12B	R71	5A	U14	11A
J24	12B	R72	2A	U15	10A
J25	11D	R73	2A	U16	10B
J26	12B			U17	11C
		U3C	10D	U18	10C
P1	15D, 2D	U5A	7A	U20	7C
		U6A	10D	U26	6B
R8	8D	U6B	10C	U27	6C
R14	6A	U6C	9D	U30	14B
R15	8A	U6D	9D	U31	14A
				U32A	12A
				U32B	13A
				U33A	15C
				U33C	15A
				U34A	14C
				U34C	14D
				U34D	14D
				U35A	15A
				U35B	15A
				U36A	5A
				U36B	5A
				U37A	3A
				U37B	3A
				U38A	14D
				U38C	5B
				U38D	5C
				U39	3B
				U40A	4A
				U40B	4B
				U41A	4C
				U41B	4C
				U43	6D



Original

Figure FO 5-13. Controller Module A1A8, Schematic Diagram (Sheet 2 of 2)

GENERAL NOTES

A. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS, 1/4 WATT.
CAPACITANCE VALUES ARE IN MICROFARADS.

B. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

CIRCUIT GROUND

PULLUP

TO

FROM

TEST POINT

CHASSIS GROUND

PARTS LOCATION INDEX

A2A1DS1	5A	A2A1A1S01	7D	A2A1A1S30	6D	A2A1A1S61	5D
DS2	5A	S02	7D	S31	6D	S62	5D
DS3	6A	S03	7D	S32	6D	S63	5D
DS4	6A	S04	7D	S33	6D	S64	5D
DS5	6A	S05	7D	S34	6D	S65	5D
		S06	7D	S35	6D	S66	5D
S1	8C	S07	7C	S36	6D	S67	5C
S2	8B	S10	6D	S37	6C	S70	5D
		S11	6D	S40	6D	S71	5D
A2A1A1E1	5A	S12	6D	S41	6D	S72	5D
E2	5A	S13	6D	S42	6D	S73	5D
E3	5A	S14	6D	S43	6D	S74	5D
E4	5A	S15	6D	S44	6D	S75	5D
E5	5A	S16	6D	S45	6D	S76	5D
E6	6A	S17	6C	S46	6D	S80	6B
E7	6A	S18	6D	S47	6C	S81	6B
E8	6A	S19	6D	S50	6D	S82	6B
E9	6A	S20	6D	S51	6D	S83	6B
E10	6A	S21	6D	S52	6D	S84	5B
E11	6A	S22	6D	S53	6D	S86	5B
E12	6A	S23	6D	S54	6D		
E13	7B	S24	6D	S55	6D	A2A1A2P1	1D
E14	7B	S25	6D	S56	6D		
		S26	6D	S57	6C	XA1J1	3D
R1	7C	S27	6C	S60	5D	XA1J1	3D
P1	3D						
P2	3B						

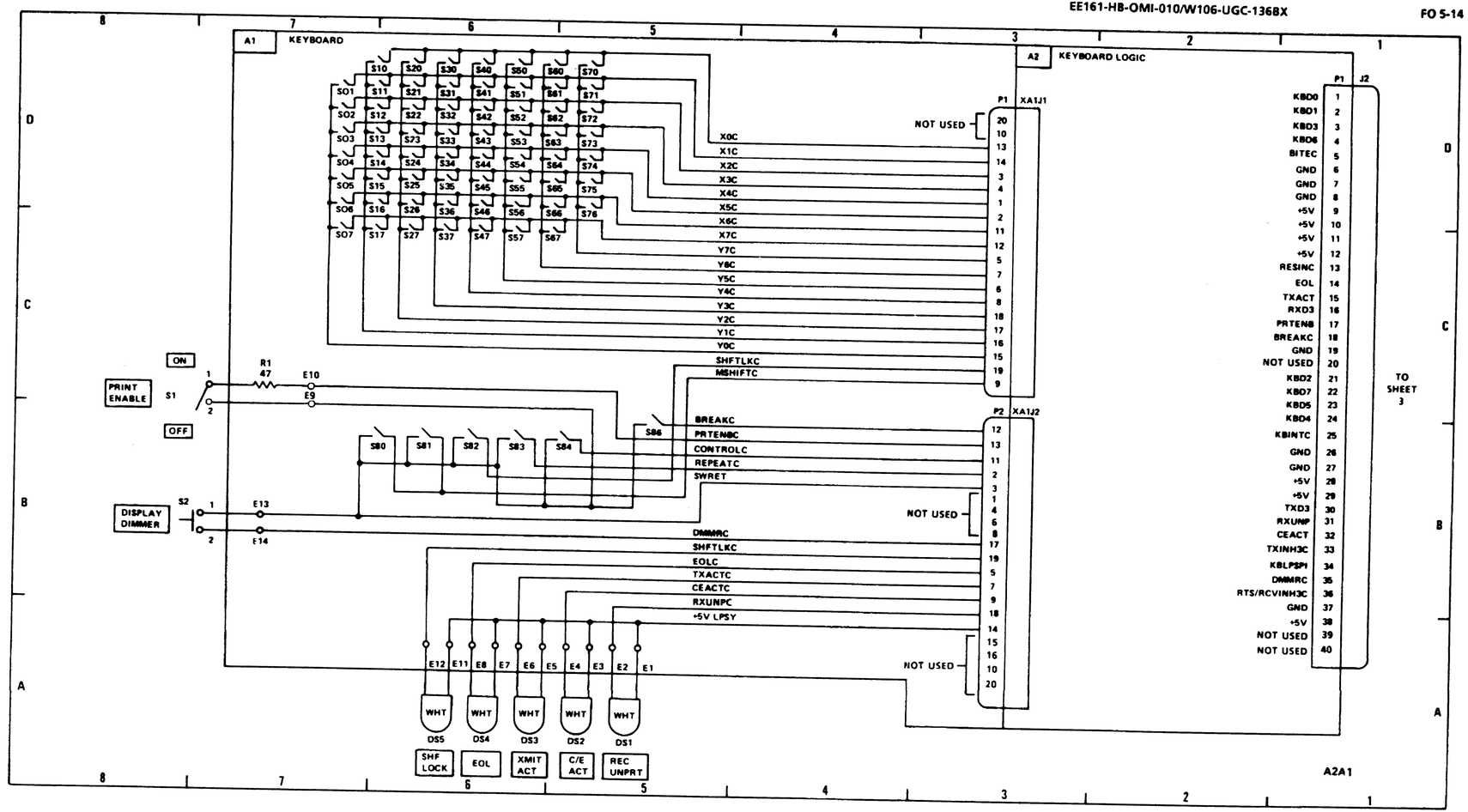


Figure FO 5-14. Keyboard Module (A2A1), Schematic Diagram (Sheet 1 of 3)

PARTS LOCATION INDEX

A2A1A2C1	13B	A2A1A2R4	6A
C2	11C	R5	6A
C3	12B	R6	13A
C4	12A	R7	4C
C5	12D		
C6	3D	TP1	4C
C6	3D	TP2	2B
C7	5D		
C8	2A	U1	13C
		U2	4A
J1	14D	U3	4B
	9B	U4	4B
		U5	12B
J2	14B	U6	13D
	7B	U7	4D
		U8	5D
P1	1D	U9A	3B
		U9B	4B
R1	6A	U9D	7C
R2	5A	U10	10D
R3	6A	Y1	12B

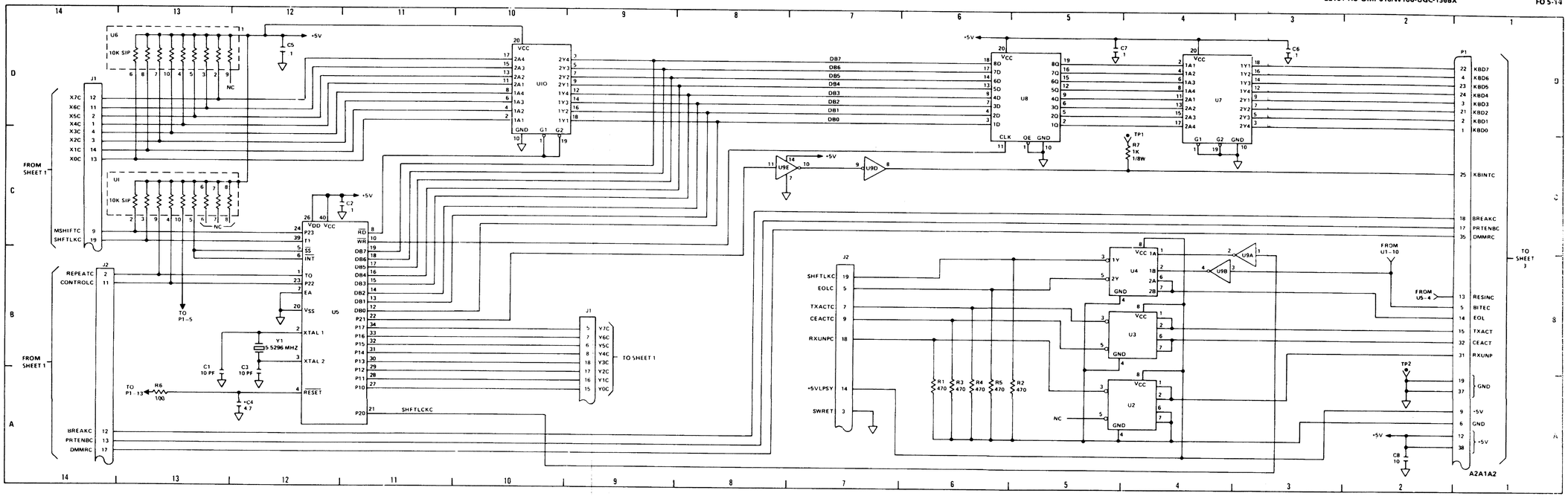


Figure FO 5-14. Keyboard Module (A2A1), Schematic Diagram (Sheet 2 of 3)

KEYBOARD MODULE ASSY A2A1
KEYBOARD LOGIC A2A1A2
(SHEET 1)

KEYBOARD A2

J1

KBD0	1
KBD1	2
KBD3	3
KBD6	4
BITEC	5
GND	6
GND	7
GND	8
+5V	9
+5V	10
+5V	11
+5V	12
RESINC	13
EOL	14
TXACT	15
RXD3	16
PRTENB	17
BREAKC	18
GND	19
	20
KBD2	21
KBD7	22
KBD5	23
KBD4	24
KBINTC	25
GND	26
GND	27
+5V	28
+5V	29
TXD3	30
RXUNP	31
CEACT	32
TXINH3C	33
KBDPSP1	34
DMMRC	35
RTS/RCVINH3C	36
GND	37
+5V	38

P1

1	KBD0
2	KBD1
3	KBD3
4	KBD6
5	BITEC
6	GND
7	GND
8	GND
9	+5V
10	+5V
11	+5V
12	+5V
13	RESINC
14	EOL
15	TXACT
16	RXD3
17	PRTENB
18	BREAKC
19	GND
20	KBD2
21	KBD7
22	KBD5
23	KBD4
24	KBINTC
25	GND
26	GND
27	+5V
28	+5V
29	TXD3
30	RXUNP
31	CEACT
32	TXINH3C
33	KBLPSP1
34	DMMRC
35	RTS/RCVINH3C
36	GND
37	+5V

TO SHEET 2

J1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37

P1

1-LINE DISPLAY A2A2 (FO 5-15)

A2A1

Figure FO 5-14. Keyboard Module (A2A1), Schematic Diagram (Sheet 3 of 3)

GENERAL NOTES

A. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS, 1/4 WATT.
CAPACITANCE VALUES ARE IN MICROFARADS.

B. COMMON CONNECTION AND CIRCUIT CONNECTION SYMBOLS ARE AS FOLLOWS:

CIRCUIT GROUND

PULLUP

TO

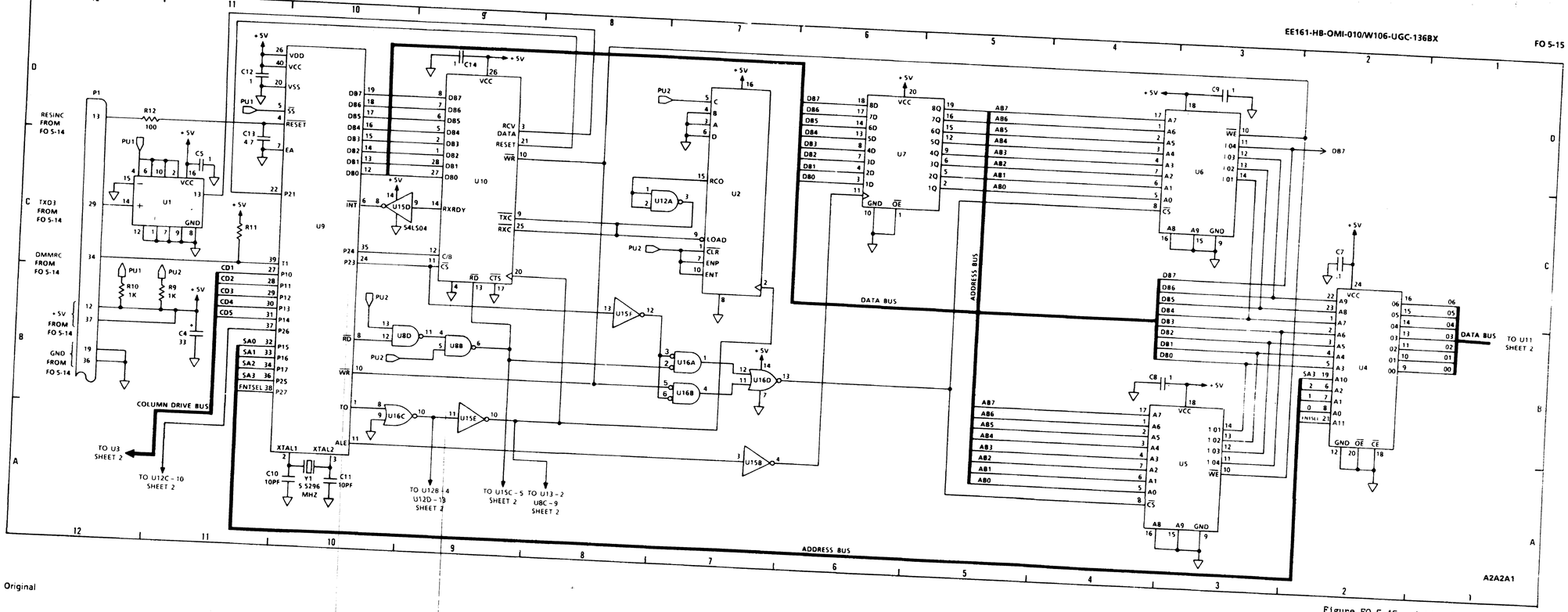
FROM

TEST POINT

CHASSIS GROUND

PARTS LOCATION INDEX

A2A2A1C4	11B	A2A2A1U4	2B
C5	11C	U5	3B
C7	2C	U6	3D
C8	4B	U7	6D
C9	3D	U8B	9B
C10	10A	U8D	9B
C11	10A	U9	10C
C12	11D	U10	9C
C13	11C	U12A	8C
C14	9D	U15B	7A
		U15D	10C
P1	12D	U15E	9A
		U15F	8B
R9	11B	U16A	7B
R10	12B	U16B	7B
R11	11C	U16C	10A
R12	12D	U16D	7B
U1	11C		
U2	7C	Y1	10A



Original

Figure FO 5-15. 1-Line Display (A2A2), Schematic Diagram (Sheet 1 of 4)

PARTS LOCATION INDEX

A2A2A1C1	9A	A2A2A1R1	11B
C2	8A	R2	12C
C3	8A	R3	12C
C6	3B	R4	11C
C15	8D	R5	12B
C16	6D	R6	11B
C17	3D	R7	11A
C18	3C	R8	10A
C19	3C	R13	11B
C20	2D	R14	12B
		R15	11B
P1	13C	R16	12B
		R17	2D
Q1	11C	U3	3B
Q2	11C	U8A	2D
Q3	11B	U8C	4B
Q4	11A	U11	8C
Q5	10A	U12B	8D
Q6	10C	U12C	4C
Q7	10B	U12D	4D
Q8	10B	U13	6C
Q9	10B	U14A	4C
Q10	10B	U14B	4B
Q11	11B	U15A	5C
Q12	11B	U15C	7D

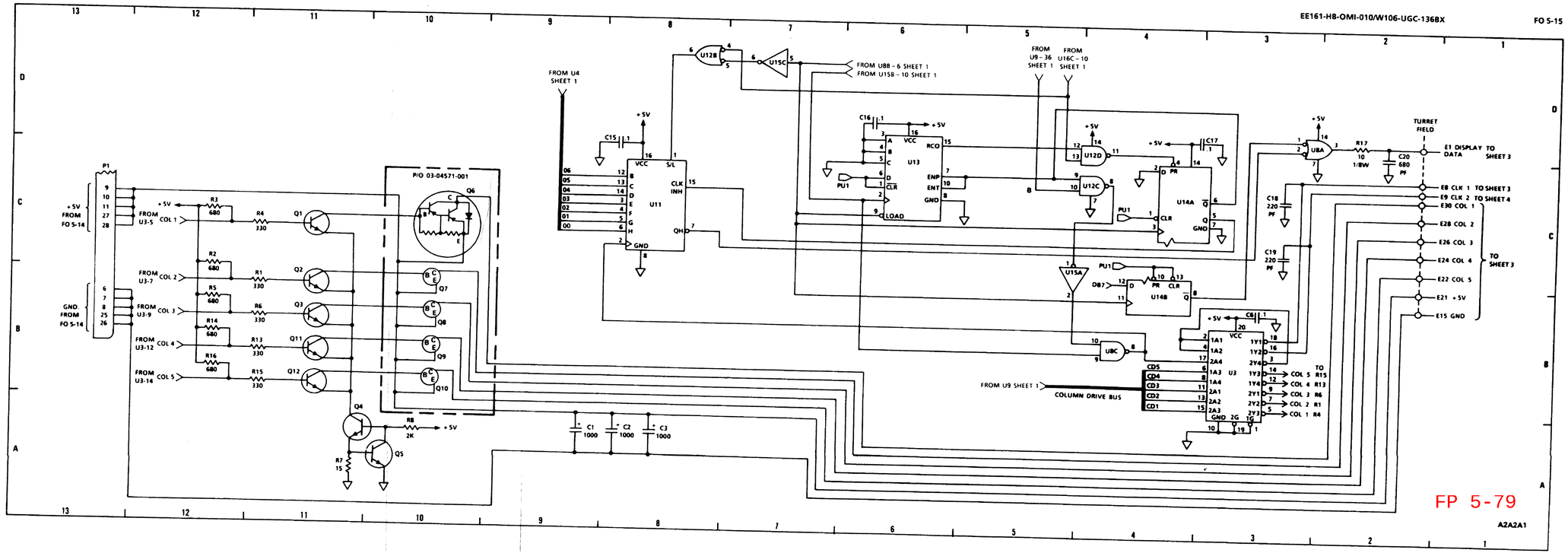


Figure FO 5-15. 1-Line Display (A2A2), Schematic Diagram (Sheet 2 of 4)

Original

PARTS LOCATION INDEX

A2A2A1C1	10C
C2	5C
C3	8A
E1	11C
E8	11B
E14	11B
E20	11B
E22	11D
E24	11D
E26	11D
E28	11D
E30	11D
U1	10C
U2	9C
U3	7C
U4	5C
U5	3C
U6	10B
U7	9B
U8	7B
U9	5B
U10	3B

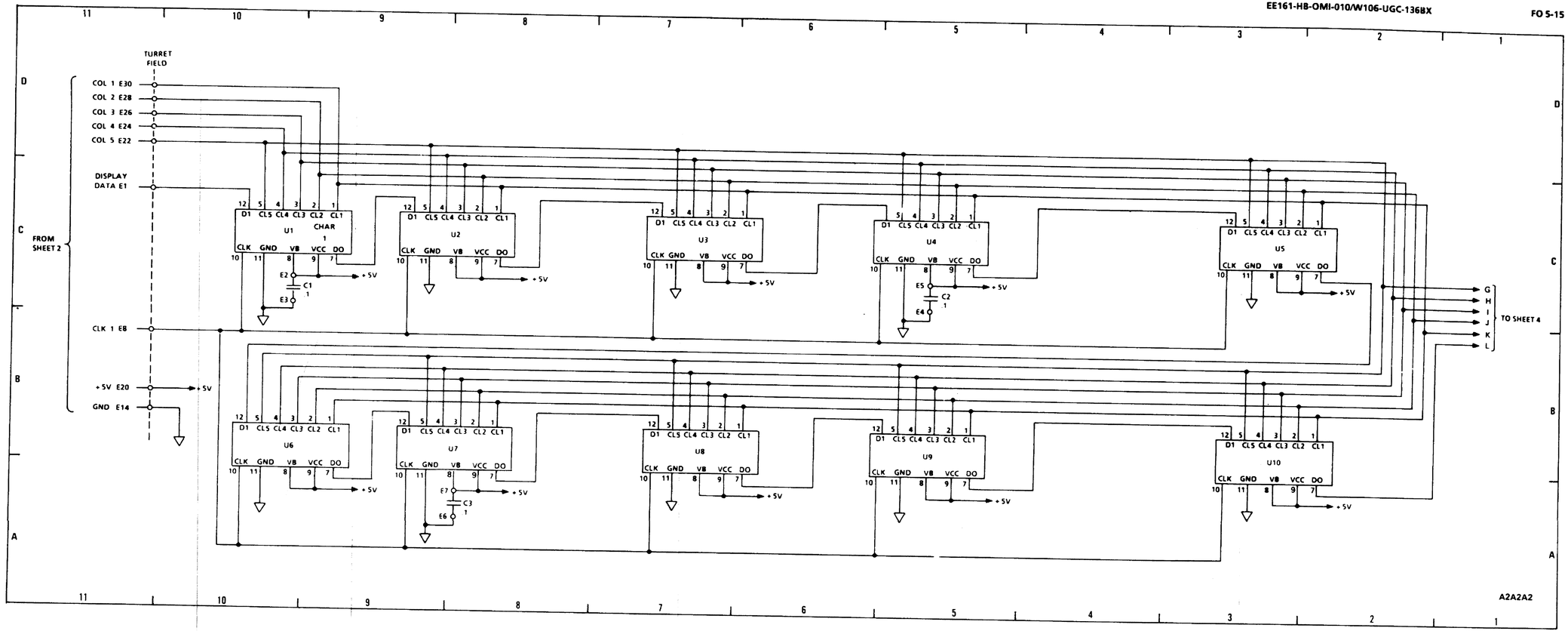


Figure FO 5-15. 1-Line Display (A2A2), Schematic Diagram (Sheet 3 of 4)

Original

PARTS LOCATION INDEX

A2A2A2C4	9C
C5	6C
C6	2A
C7	6B
E9	10C
U11	9C
U12	8C
U13	6C
U14	4C
U15	2C
U16	9B
U17	8B
U18	6B
U19	4B
U20	2B

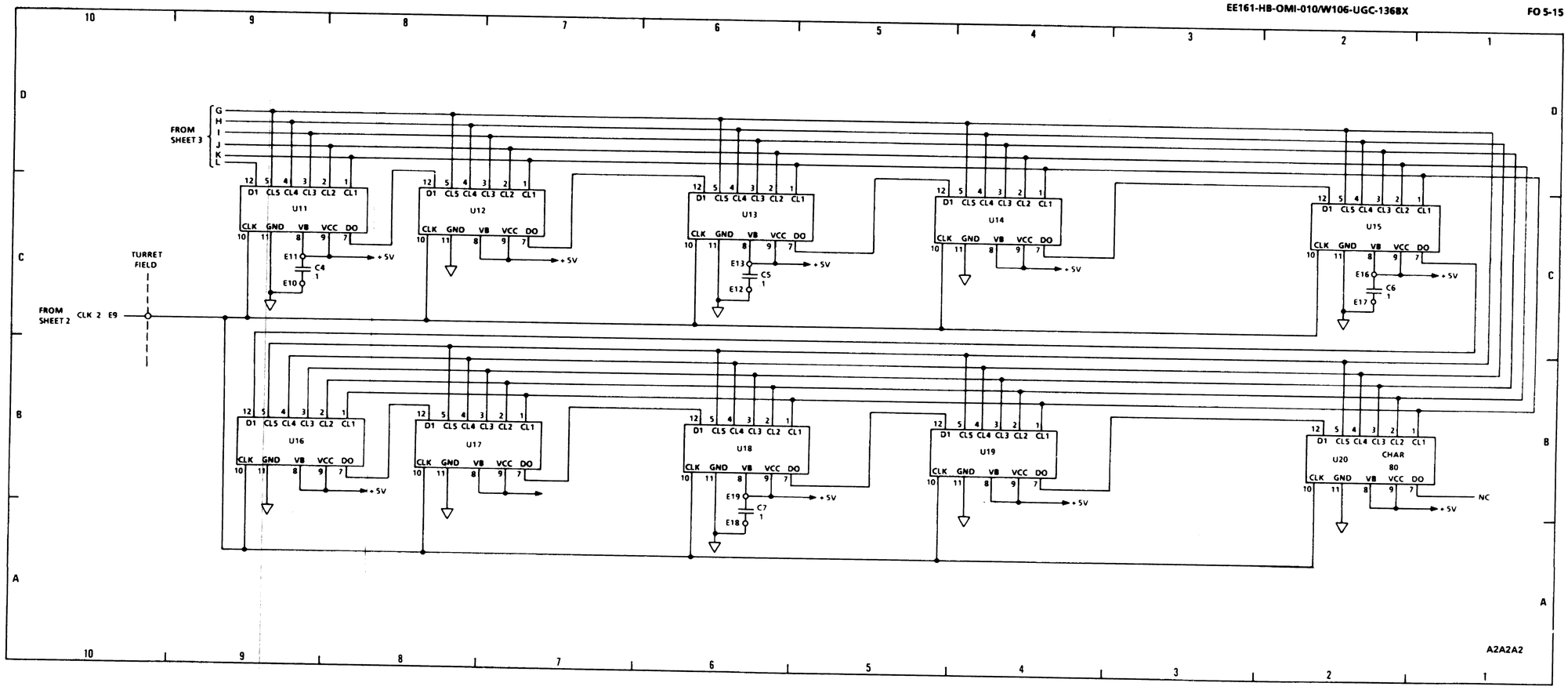


Figure FO 5-15. 1-Line Display (A2A2), Schematic Diagram (Sheet 4 of 4)

GENERAL NOTES

A. [ ] INDICATES FRONT PANEL MARKINGS.

B. KEY

———YES

— — —NO

SPECIFIC NOTES

1. THE LAMP TEST CONSISTS OF THE PAPER LOW, PARITY, EOL, XMIT ACT, C E ACT, AND REC UNPRT LAMPS LIGHTING AND THE EOL ALARM SOUNDS.

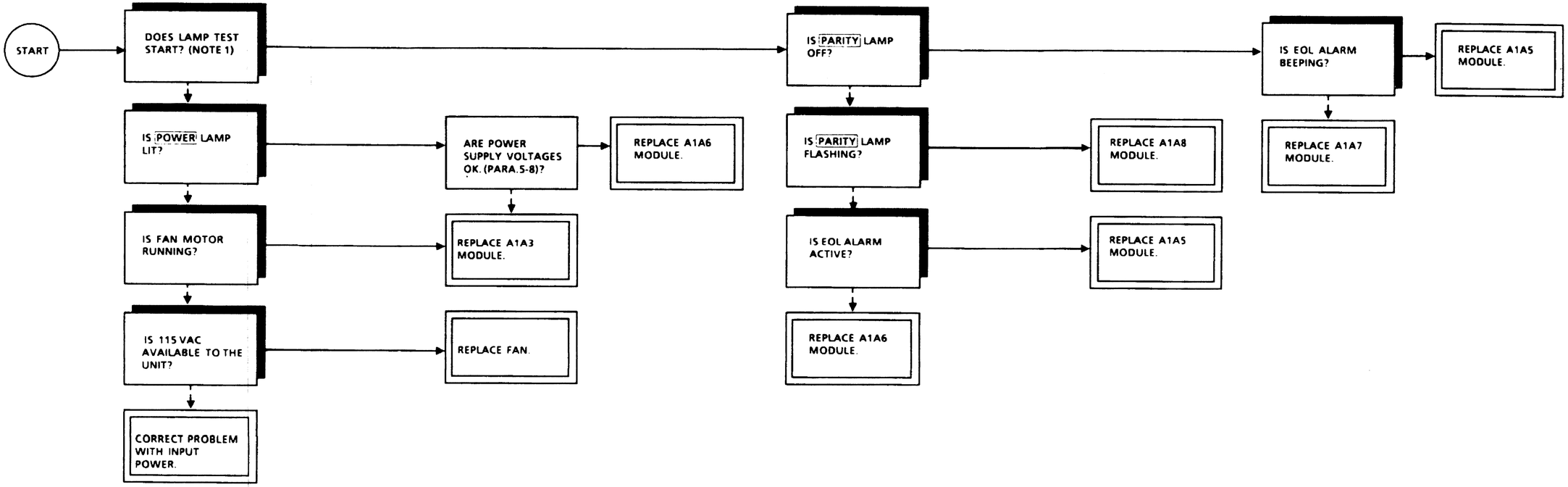
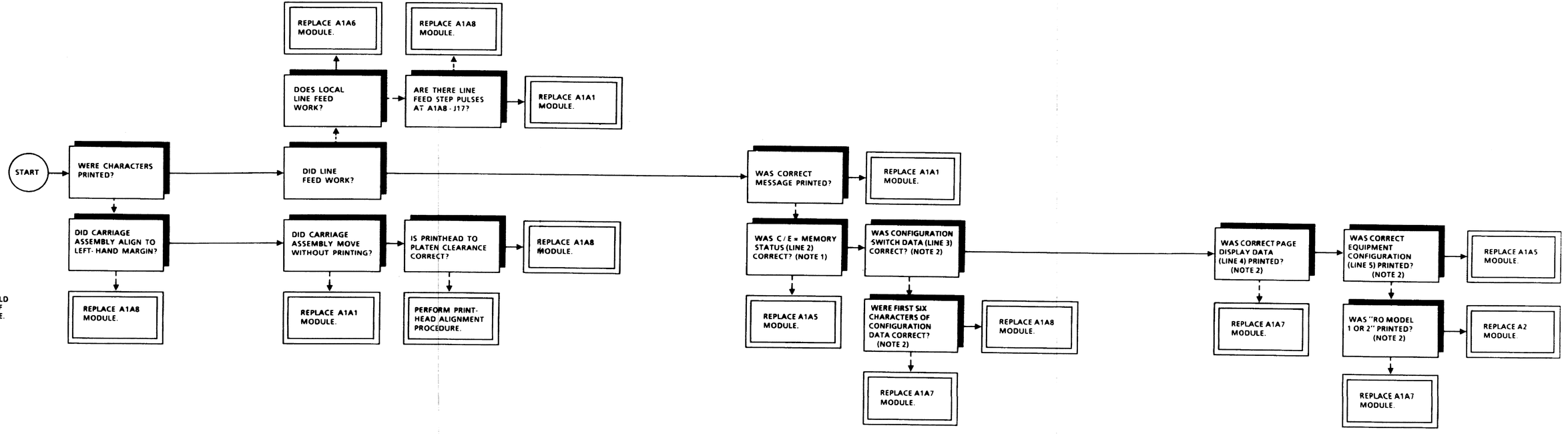


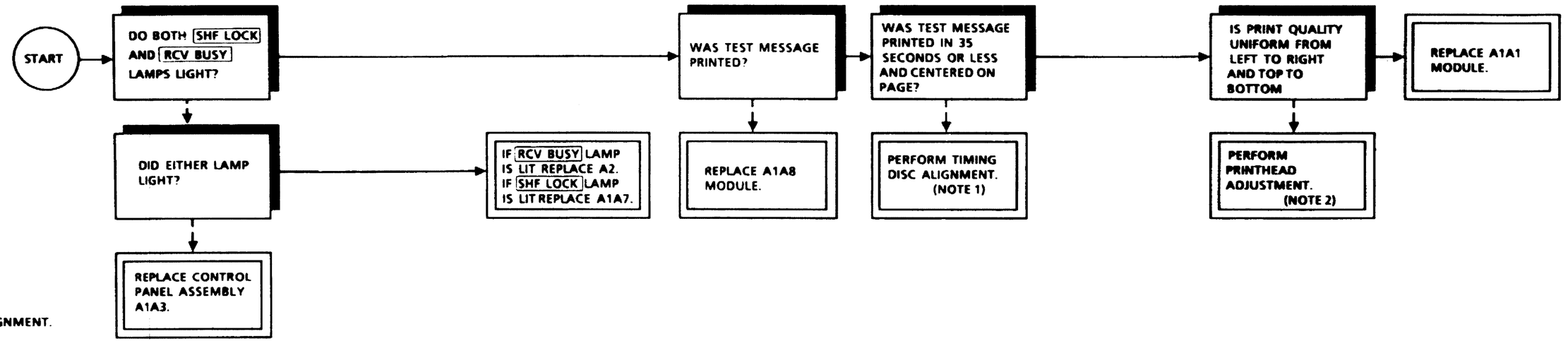
Figure FO 5-16. Power - on, Fault Isolation Diagram



GENERAL NOTES
A. KEY
——— YES
— — — NO

SPECIFIC NOTES
1. MEMORY STATUS SHOULD INDICATE 256 BLOCKS OF MEMORY ARE AVAILABLE.
2. SEE APPENDIX.

Figure FO 5-17. Intialization, Fault Isolation Diagram



GENERAL NOTES

A. [ ] INDICATES FRONT PANEL MARKINGS.

B. KEY
———YES
– – –NO

SPECIFIC NOTES

1. REFER TO PARA. 6-3.2 FOR TIMING DISC ALIGNMENT.

2. REFER TO PARA. 6-2.2 FOR PRINTHEAD ADJUSTMENT.

Figure FO 5-18. Bite, Fault Isolation Diagram

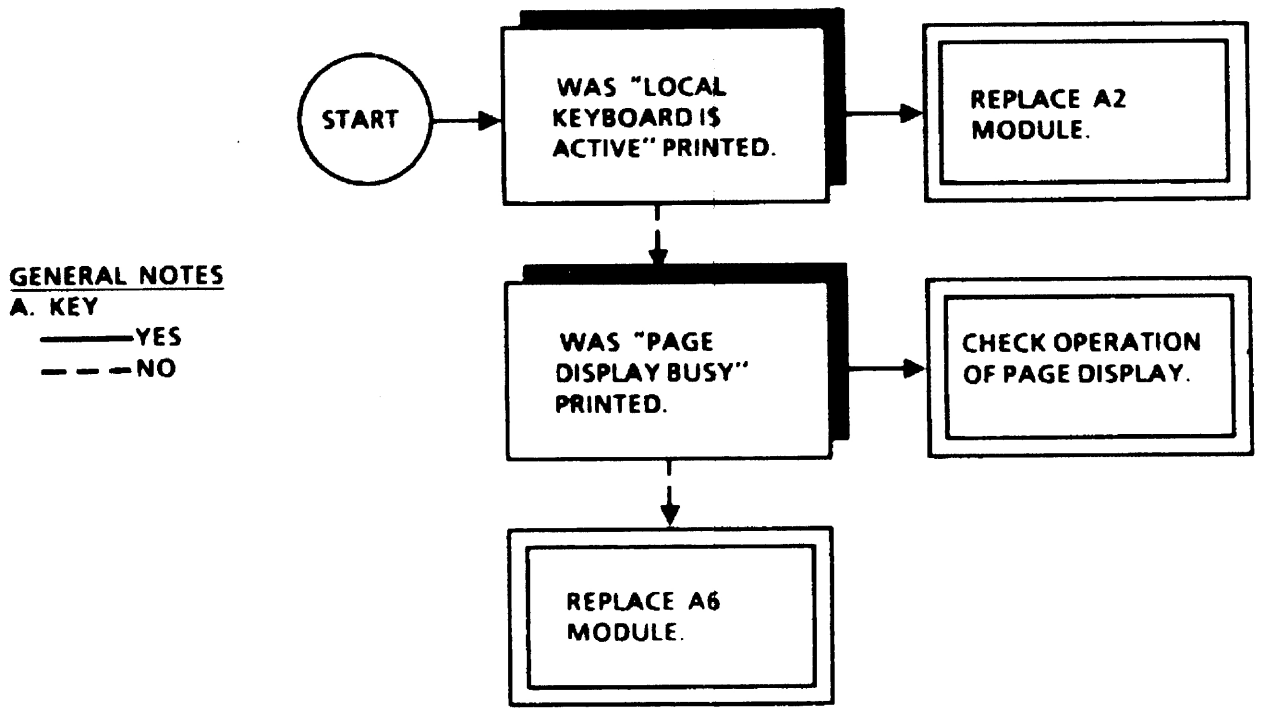


Figure FO 5-19. Compose/Edit, Fault Isolation Diagram

CAUTION
DAMAGE WILL RESULT TO EQUIPMENT IF POWER IS APPLIED TO PRINT MECHANISM BEFORE ZENER DIODES ARE CHECKED.

GENERAL NOTES
A. ☐ INDICATES FRONT PANEL MARKINGS.
B. KEY
———YES
— — —NO

SPECIFIC NOTES
1. ENSURE PRINT MECHANISM IS CLEAR OF DEBRIS PRIOR TO PERFORMING FAULT ISOLATION PROCEDURE.

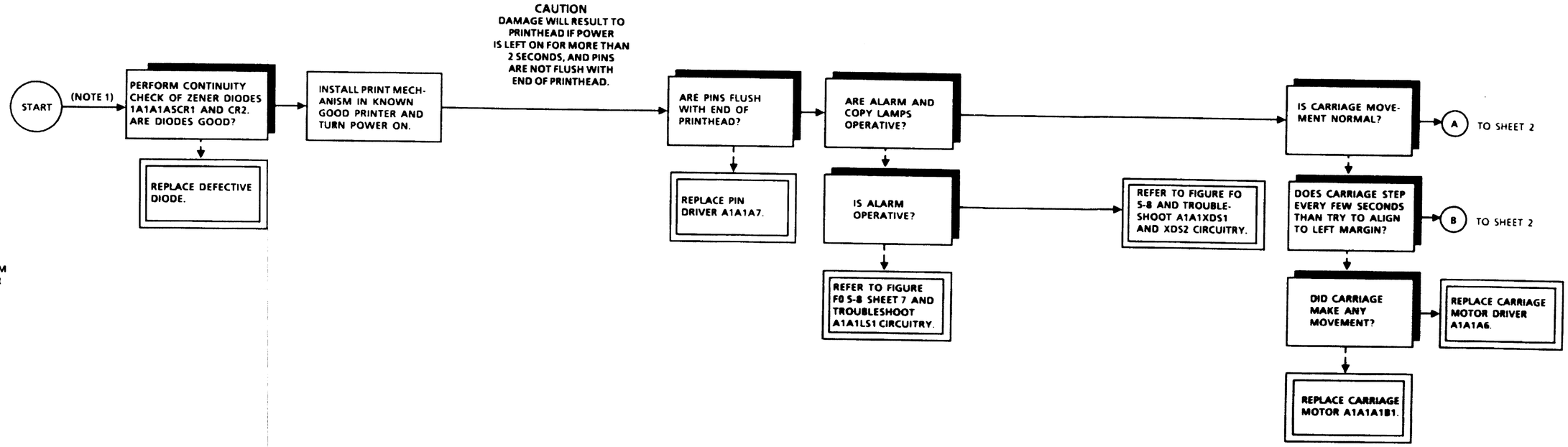


Figure FO 5-20. Print Mechanism, Fault Isolation Diagram (Sheet 1 of 3)

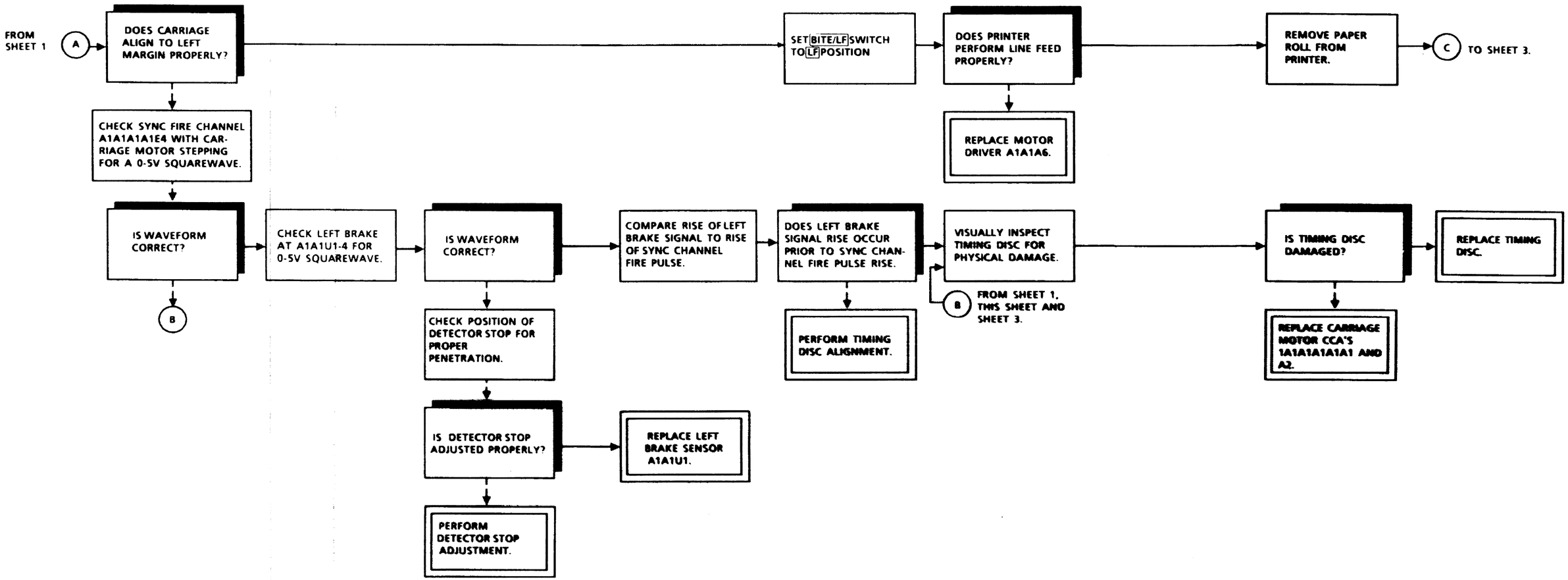


Figure FO 5-20. Print Mechanism, Fault Isolation Diagram (Sheet 2 of 3)

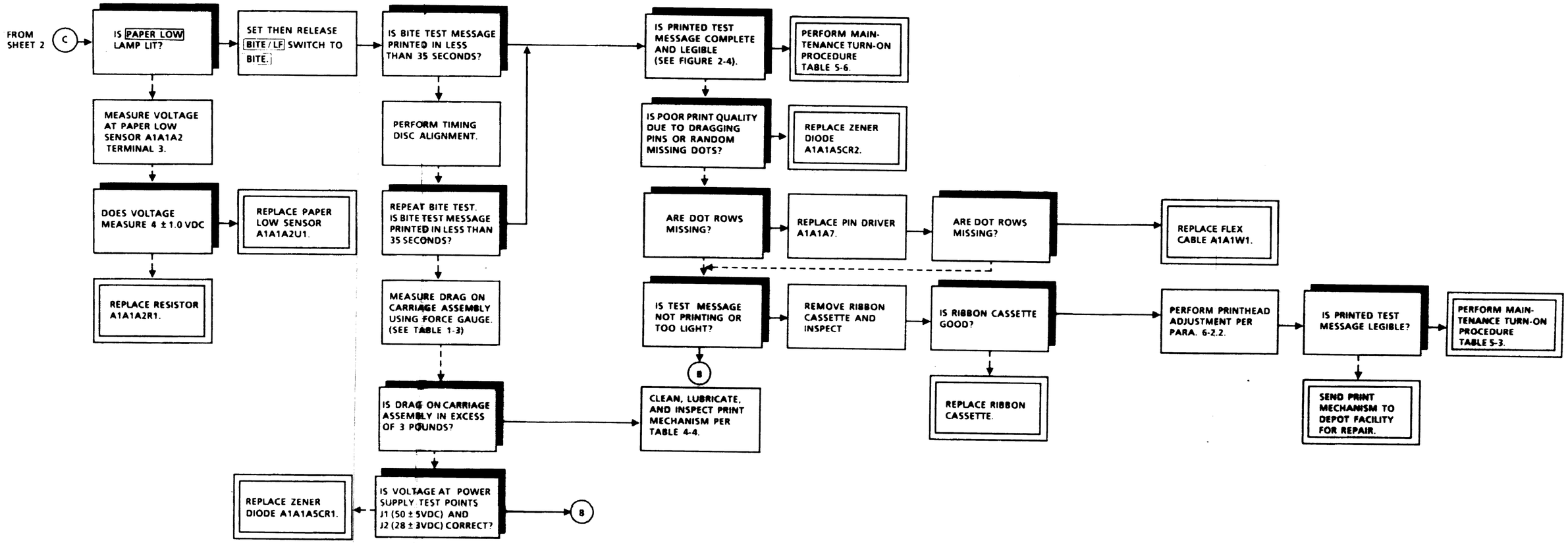


Figure FO 5-20. Print Mechanism, Fault Isolation Diagram (Sheet 3 of 3)

Original

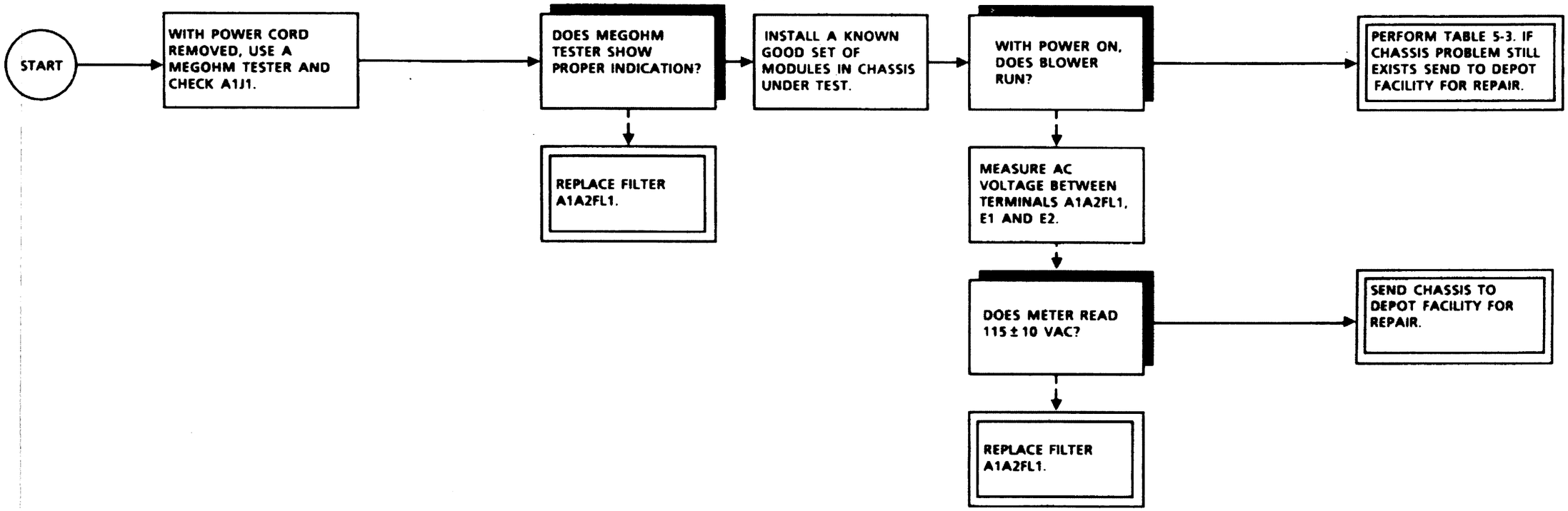


Figure FO 5-21. Teleprinter Chassis, Fault Isolation Diagram

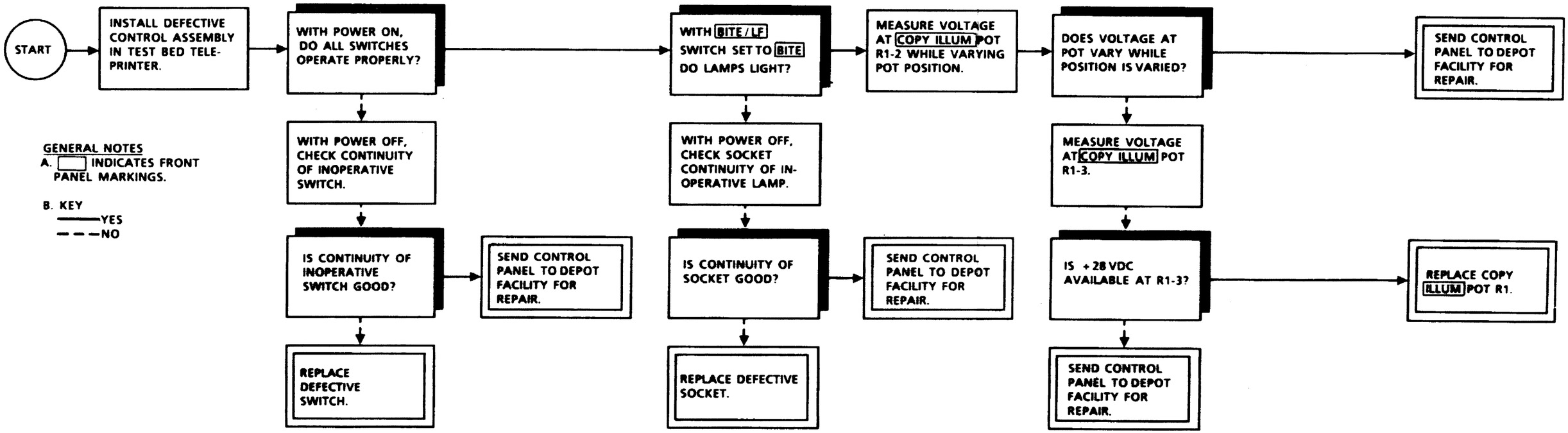


Figure FO 5-22. Control Panel, Fault Isolation Diagram