DATASPEED TAPE TO TAPE SYSTEM TYPE 1 AND TYPE 2 TAPE SENDERS AND RECEIVERS

ELECTRONIC CIRCUITRY SCHEMATIC DIAGRAMS AND CIRCUIT BOARD DRAWINGS

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1. INTRODUCTION

- 1.01 This section provides the schematic diagrams and circuit board drawings for the 1A and 2A Tape Senders and 1B and 2B Tape Receivers used in the DATASPEED Tape to Tape System. The actual wiring diagrams for the Sender and Receiver are provided in a separate section.
- 1.02 This section is reissued to rearrange text and to include the latest diagram drawing issues.

2. GENERAL

2.01 The schematic diagrams make use of circuit logic symbols to represent a group of electrical components arranged on a printed circuit board so as to perform a specific function or functions. Each logic symbol is designated by two numbers: a "Z" number, and an

"EC" number. The "Z" number denotes the physical location of the circuit board in the electronic module assembly represented by the schematic diagram. The "EC" number refers to the specific type of circuit board used in that location; one type of circuit board may be used in more than one location.

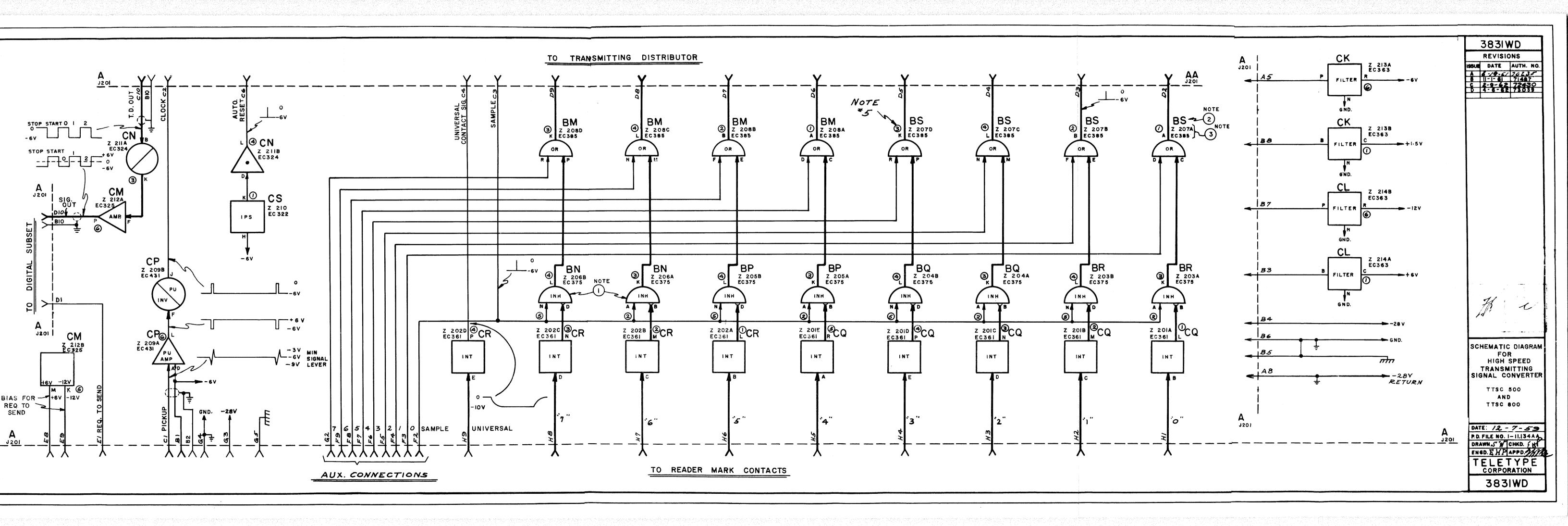
- 2.02 Each circuit board drawing carries two numbers: a six digit number, and an "EC" number. The six digit number is considered as the part number of the circuit board, and should be used (prefixed with TP) when ordering replacement circuit boards. The last three digits of the part number are the same as the three digits of the "EC" number; for example, part number TP172322 is circuit board EC322. The circuit borad drawing consists of a parts list, a parts layout of the circuit board, a schematic diagram of the circuit, a circuit description and a drawing of the circuit logic symbol.
- 2.03 The index (Part 3.) lists the subject matter of each diagram and drawing included in the section. In addition, it also lists the numbers of the WD and EC drawings. Finally, to determine which have been changed from the previous section issue, a cross-reference between section issue and diagram or drawing issue is provided.

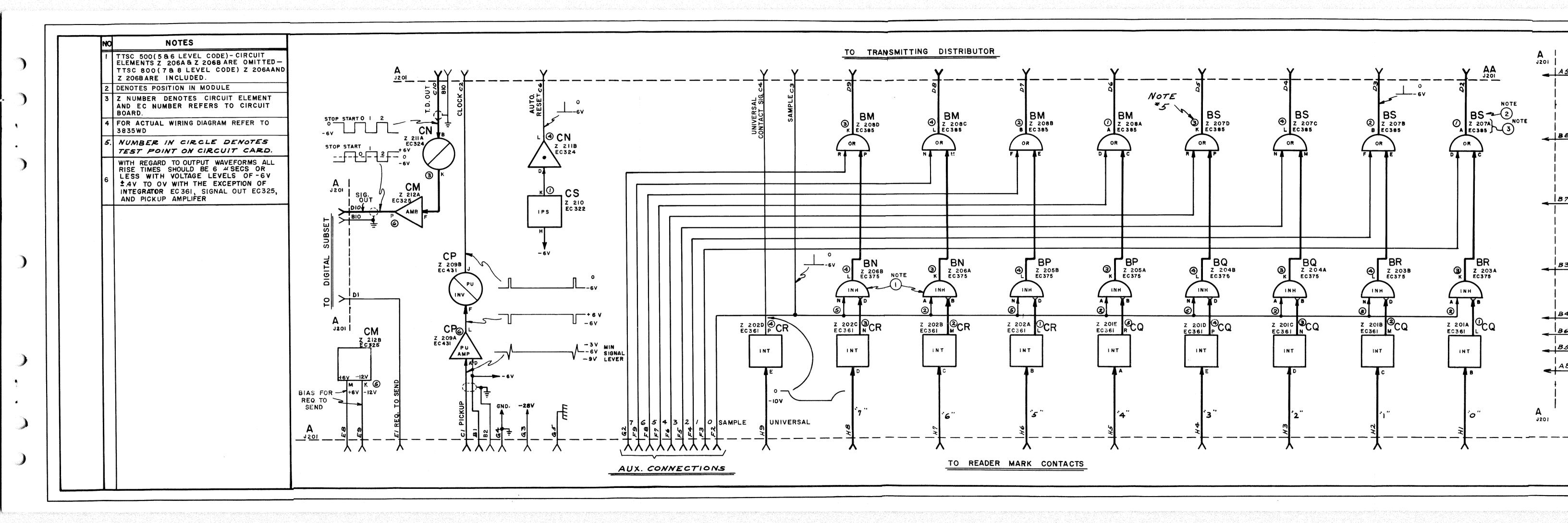
3. DIAGRAM INDEX

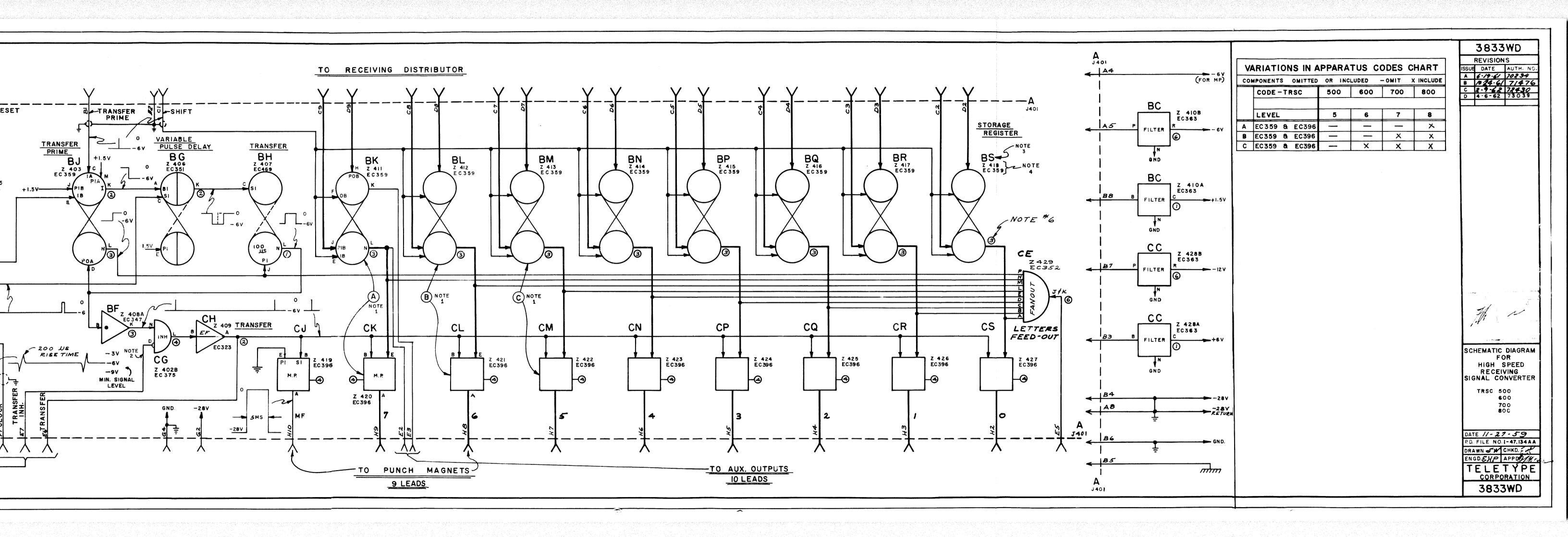
SUBJECT	DRAWING		SECTION ISSUE					
SUBJECT	NUMBER	1	2	3	4	5	6	
Sending Signal Converter Receiving Signal Converter Line Break and Automatic Answer (Sending) Automatic Answer (Receiving) Sending Distributor Receiving Distributor Y-Connector Sending Signal Converter W/Rubout Delete Relay Driver (2) Relay Driver and Receiving Input Amplifier (NPN) Emitter Follower and Inhibit Gate Integrator Pulse Shaper Symmetrical Emitter Follower Inverter and Pulse Amplifier Output Amplifier and Voltage Bias Pulse Amplifier and Emitter Follower (PNP) (NPN) Emitter Follower (2) Pulse Amplifier (2) Variable Pulse Delay (0.41 to 1.3 Milliseconds) Diode Fan-Out Gate Receiver Input Amplifier Filip-Flop Integrator Filter (2) Variable One-Shot (0.65 to 2.2 Milliseconds) Diode Gates (3) Inhibit Gate (2) Diode Gates (4) Start-Stop Oscillator (1050 Baud) Fixed One-Shot (200 Microseconds) Magnet Pulser (PNP) Inverter (2) Squaring Amplifier Pick-Up Amplifier Fixed One-Shot (100 Microseconds) Variable One-Shot (0.9 to 1.5 Milliseconds) Single Delay (50 Microseconds) Time Delay Relay Driver *Original Issue	3831WD 3833WD 3843WD 3845WD 4439WD 4441WD 4799WD 5917WD 146520 146521 172322 172323 172324 172325 172326 172333 172347 172355 172355 172355 172355 172355 172374 172361 172363 172363 172374 172375 172374 172375 172374 172375 172374 172375 172385 172396 172401 172420 172431 172469 172473 172490 177543	DD CD 322222424586325 OO3 756436439896 -	DD CF 322222424586325 OO* * * * * * * * * * * * * * * * * *	DDBOCFCA322224245873250** *** 5654644281163				

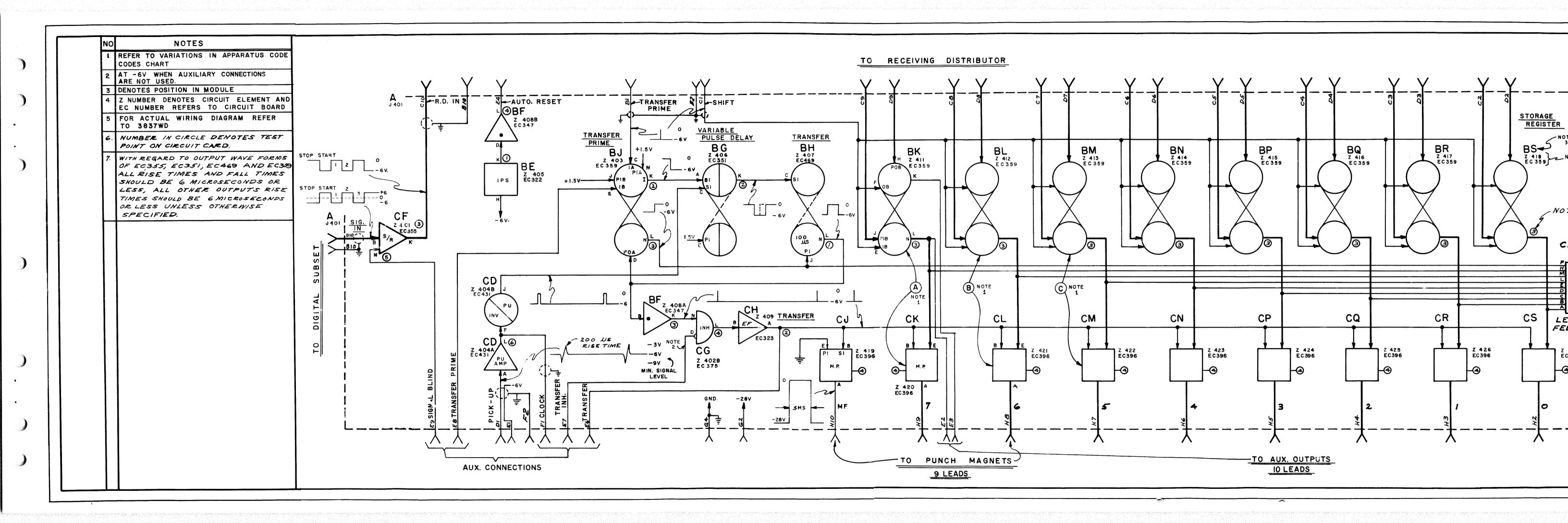
Attached: Teletype Corporation Wiring Diagrams (WD) Circuit Board Drawings (EC)

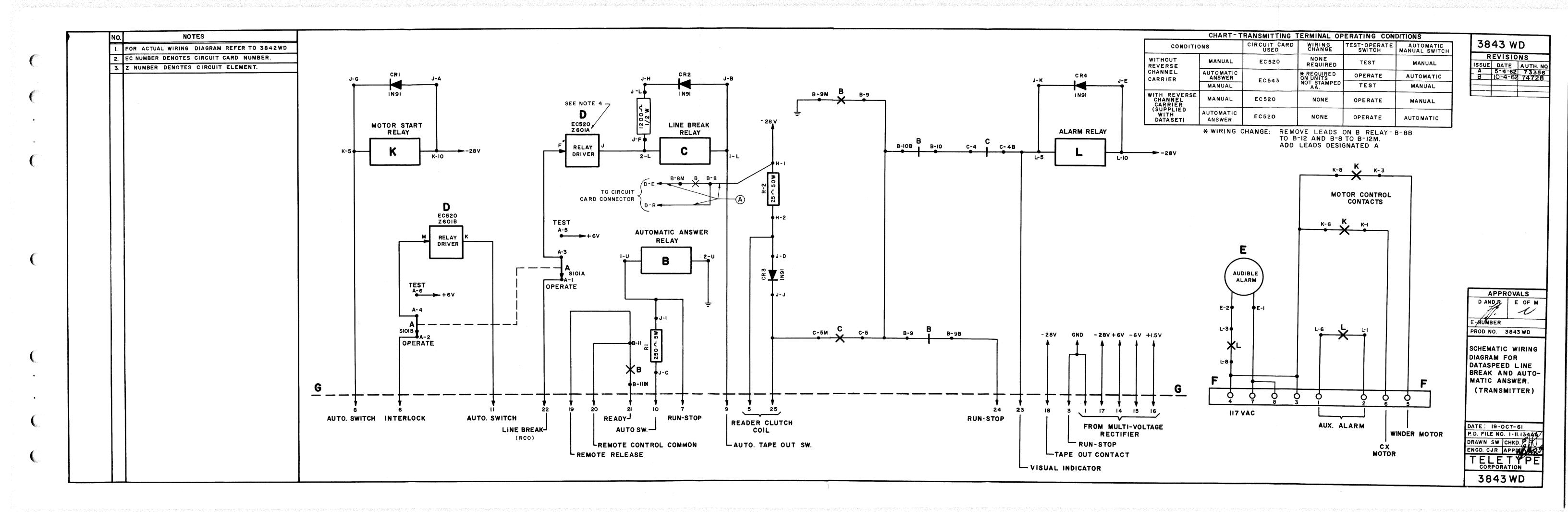
Page 2 2 Pages and Attachments

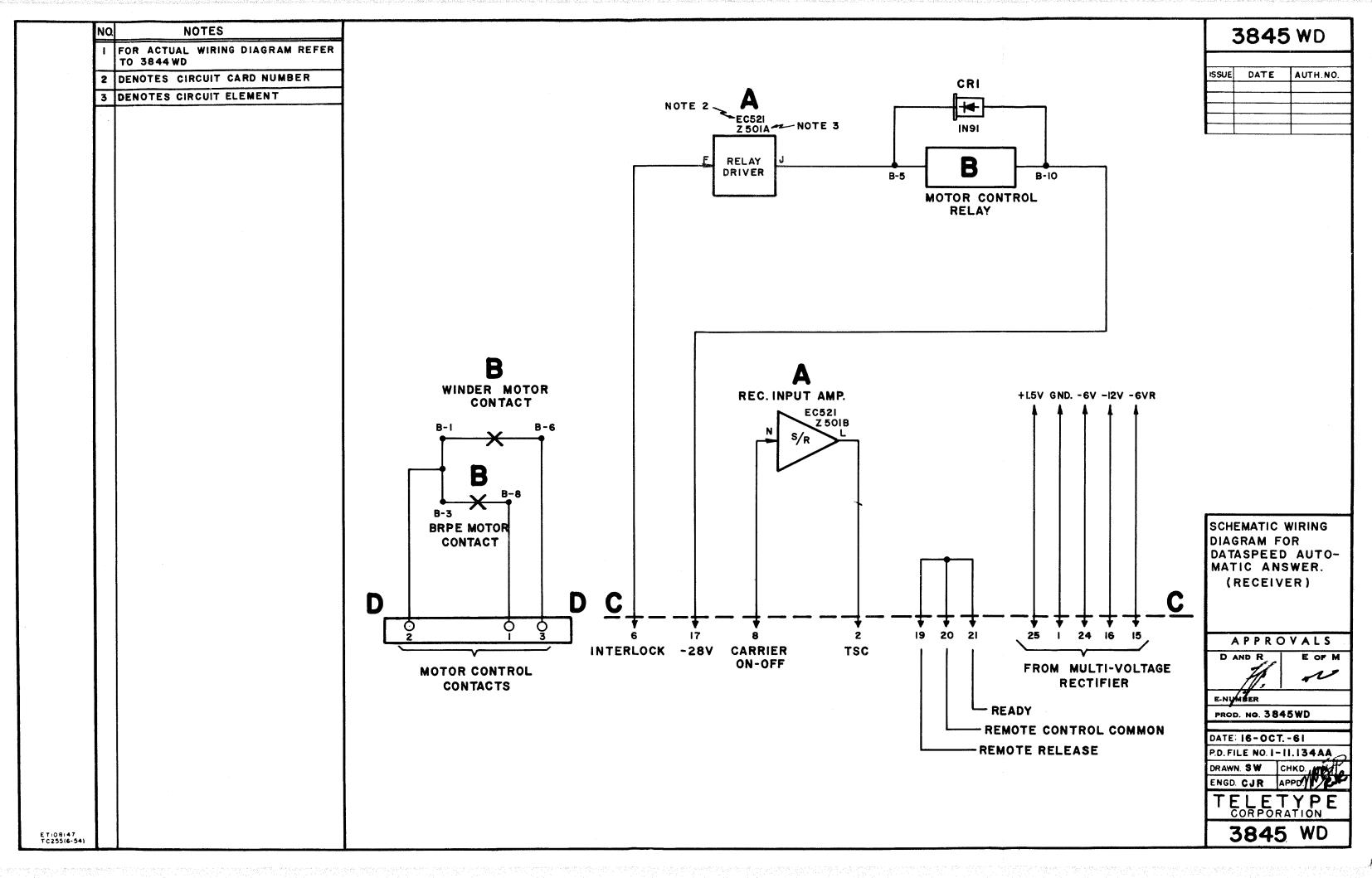


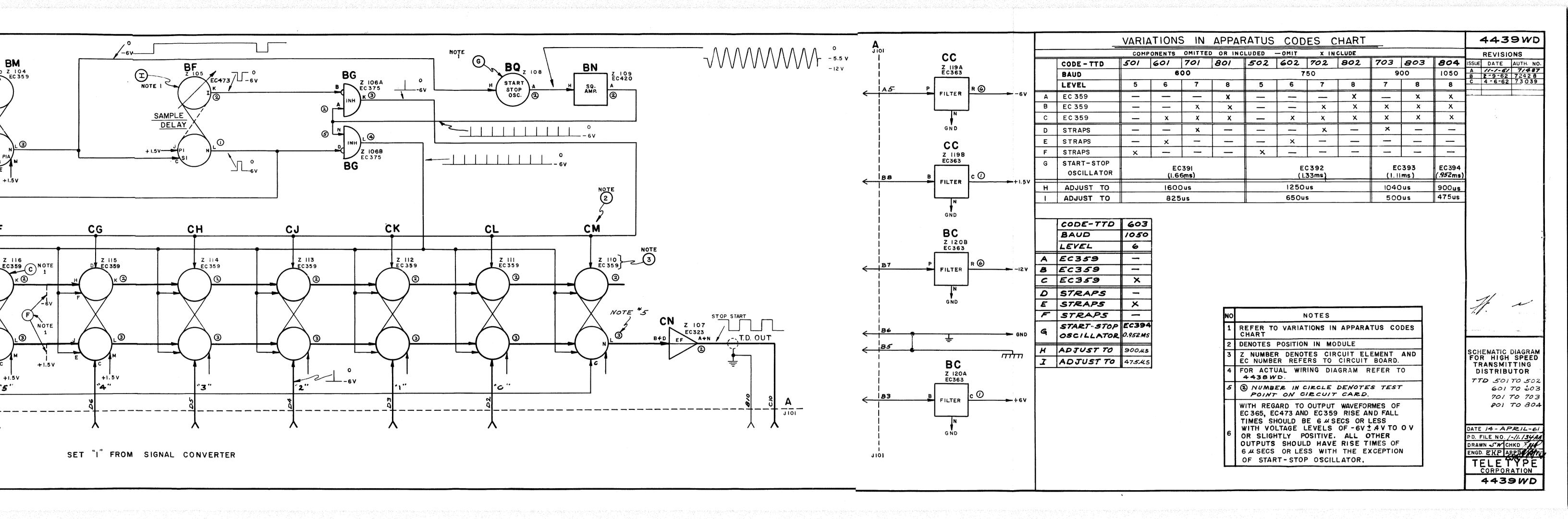


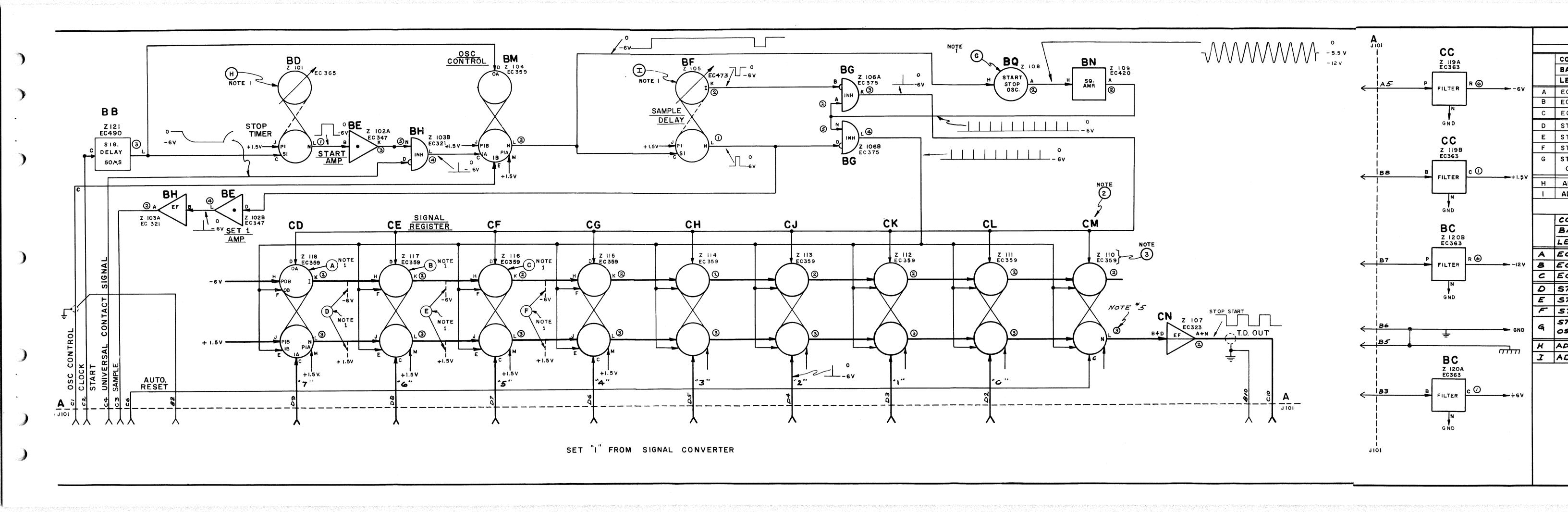


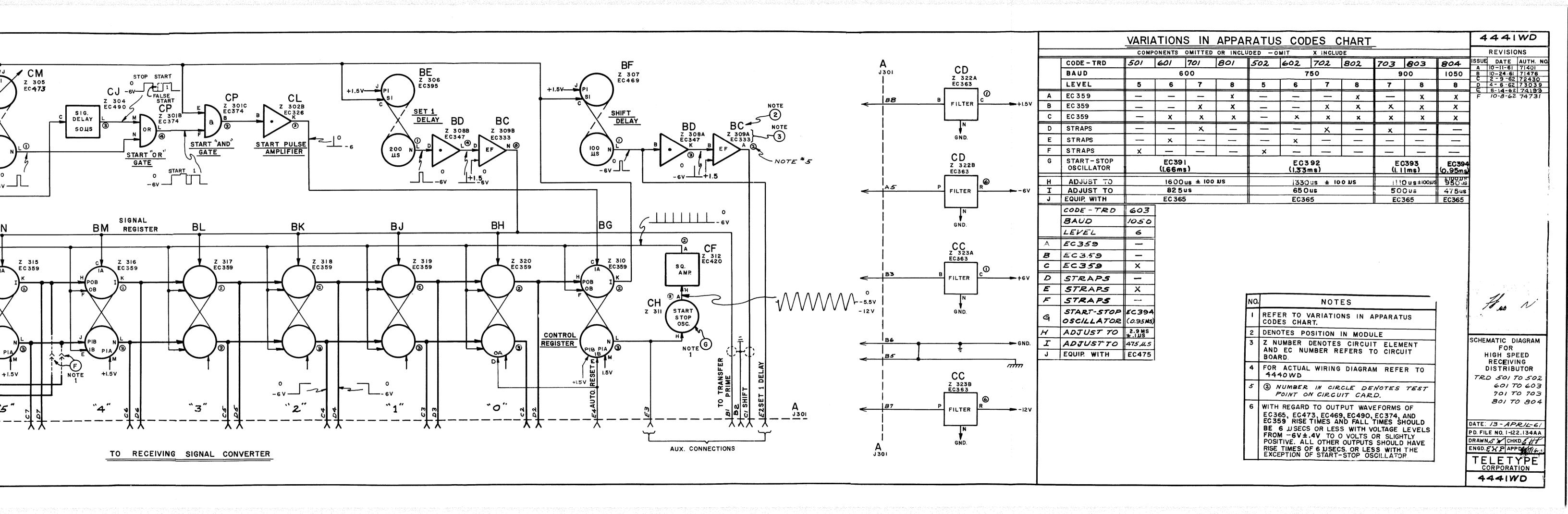


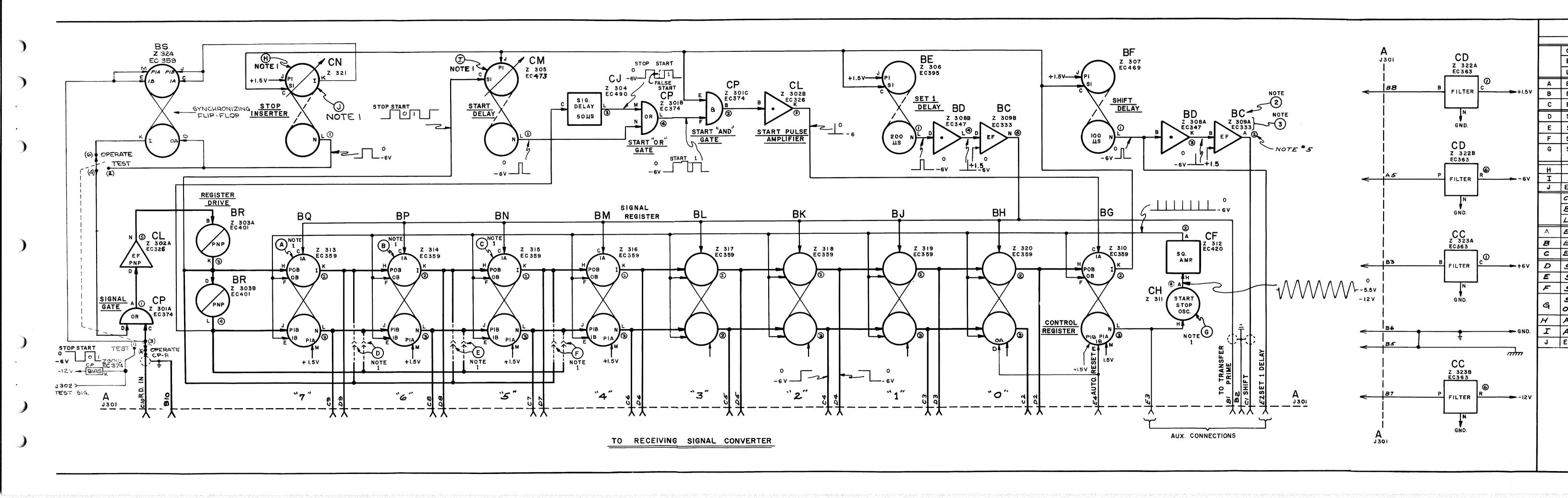


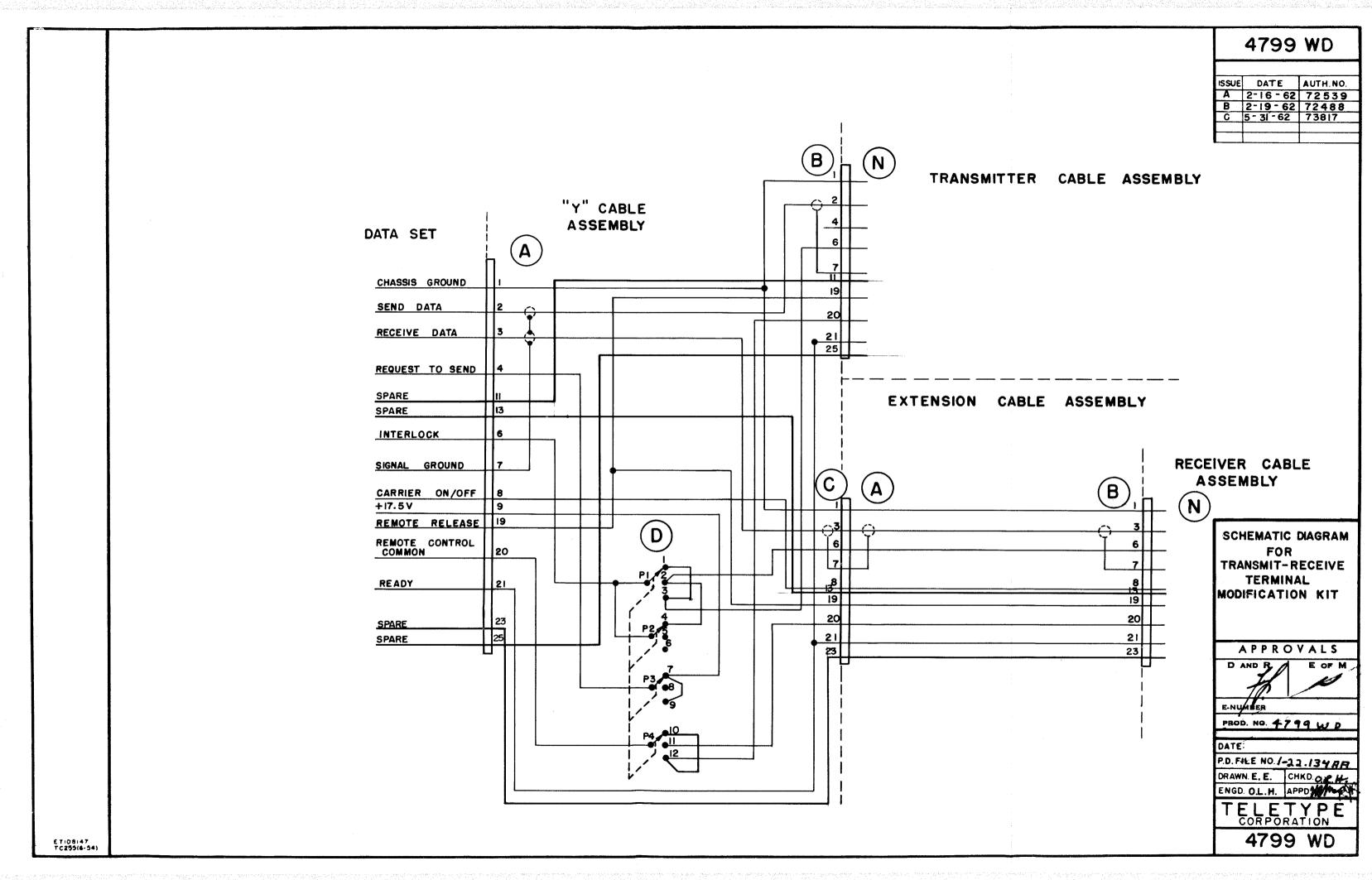


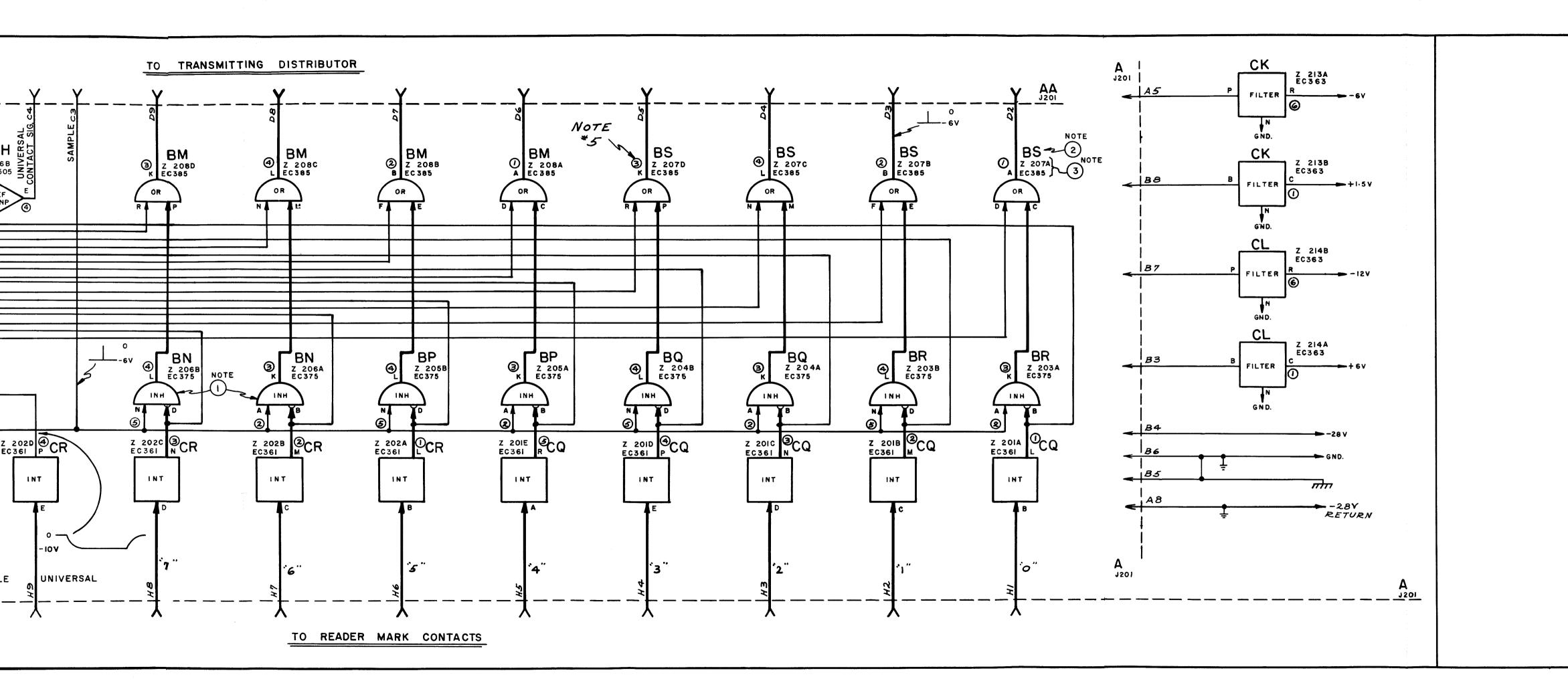










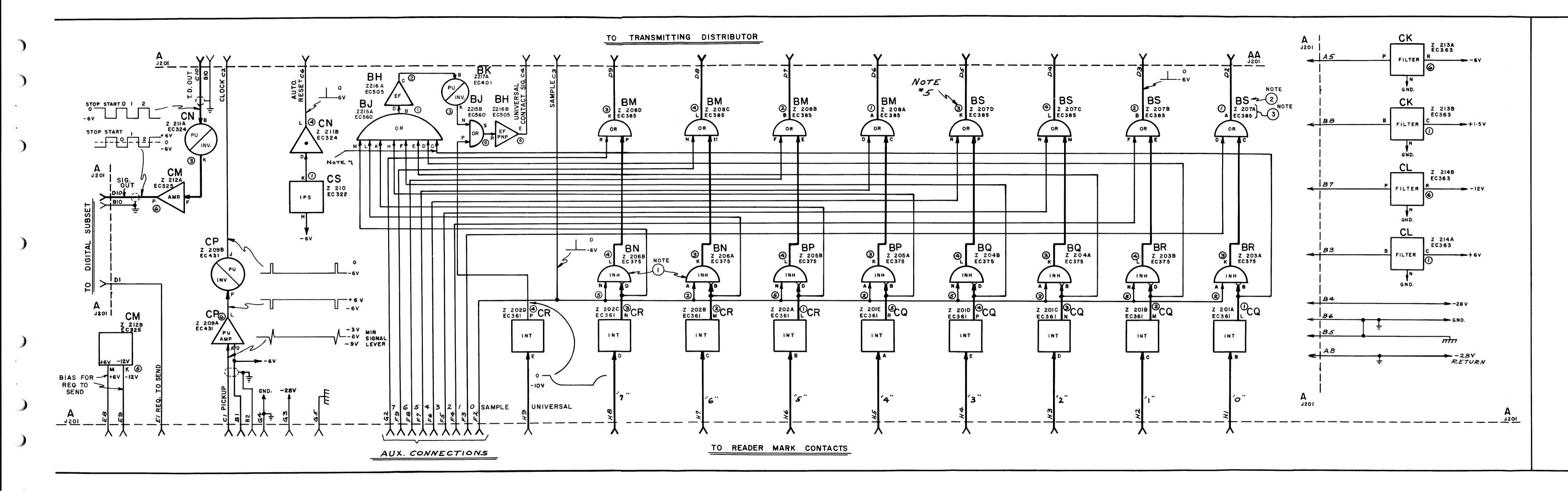


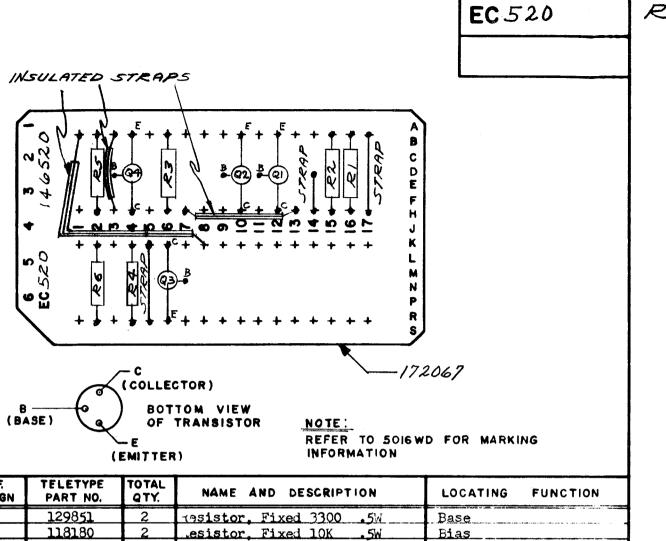
NO	NOTES
!	TTSC 501(586 LEVEL CODE)-CIRCUIT ELEMENTS Z 2068 & Z 2068 ARE OMITTED- TTSC 801(788 LEVEL CODE) Z 206AAND Z 2068 ARE INCLUDED.
2	DENOTES POSITION IN MODULE
3	Z NUMBER DENOTES CIRCUIT ELEMENT AND EC NUMBER REFERS TO CIRCUIT BOARD.
4	FOR ACTUAL WIRING DIAGRAM REFER TO 5916 WD
5.	NUMBER IN CIRCLE DENOTES TEST POINT ON CIRCUIT CARD.
6	WITH REGARD TO OUTPUT WAVEFORMS ALL RISE TIMES SHOULD BE 6 #SECS OR LESS WITH VOLTAGE LEVELS OF -6V \$.4V TO OV WITH THE EXCEPTION OF INTEGRATOR EC 361, SIGNAL OUT EC 325, AND PICKUP AMPLIFER
7.	FOR TYPE 2, 5 LEVEL OPERATION, THE LEAD ON BJ-C MUST BE REMOVED. TYPE 1, 5 LEVEL OPER- ATION IS IDENTICAL TO TYPE 2, - G,7 & B LEVEL OPERATION.

REVISIONS ISSUE DATE AUTH. NO.
A 3-/3-63 76320 SCHEMATIC DIAGRAM FOR
HIGH SPEED
TRANSMITTING
SIGNAL CONVERTER W/RUBOUT DELETE TTSC 501 AND TTSC 801 PROD. NO. 5917 WD DATE: 10-26-62 P.D. FILE NO. 1-11.134AA DRAWN SW CHKD. DE ENGD. EHP APPORTA TELETYPE CORPORATION

5917 WD

5917 WD





REF. Design	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
R1	129851	2	tasistor Fixed 3300 .5W	Base
R2	118180	2	esistor Fixed 10K .5W	Bias
R3	137442	2	esistor, Fixed 1500 .5W	Collector
R4			Same as R1	
R5			Same as R3	
R6			Same as R2	
_1	177105	2	Transistor P-22	Amolifier
.2	177224	2	Transistor 2N398 A	Power
<u>C3</u>			Same as Ul	
<u></u> 4		.	Same as Q2	
£C	172067	1	Circuit Card Etched	
		3	Strap 24 AWG	
		3	Strap 24 AWG Insulated	
	144495	4	PAD. TRANSISTOR	
		<u> </u>		
		<u> </u>		
		<u> </u>		<u> </u>
		 		
				
		<u> </u>	 	
				

RELAY DRIVER(2)

CIRCUIT BOARD EC 520

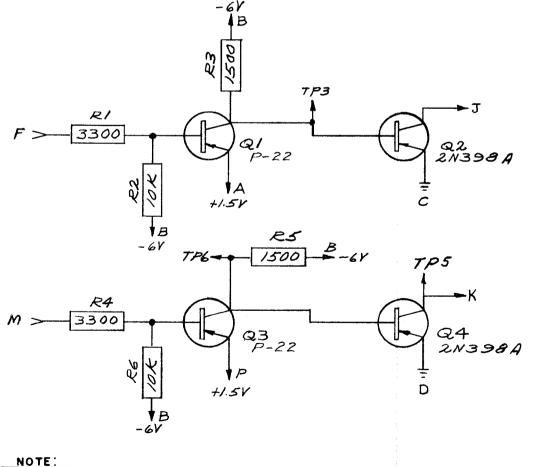
146520

This card consists of two power amplifiers which can be used as kelay Drivers. The circuits will operate with inputs of +8 and Gnd. With +8 volts at input (F), will is biased "OFF" and -6 volts appears on the base of 42, which turns "GN" and energizes the relay. With Gnd. applied at input (F), wl is biased "ON" driving 42 to cutoff by applying +1.5 volt to the base of 42. With 42 "OFF" the relay is not operated.

Relays which require operating voltages and currents greater than -30 volts and 100 ma. should not be used with these circuits.

SYMBOLS RELAY J DRIVER RELAY DRIVER

ISSUE DATE AUTH NO 2 11-29-61 71786 3 1-2-62 72087



CARD CONNECTIONS ARE REPRESENTED BY LETTERS TEST POINTS ARE REPRESENTED BY NUMBERS

E-NUMBER PROD. NO. 146520

DATE 10-007-61 PD FILE NO /-/1.134A) DRAWN 59 CHKDEH ENGO CIRE APPON

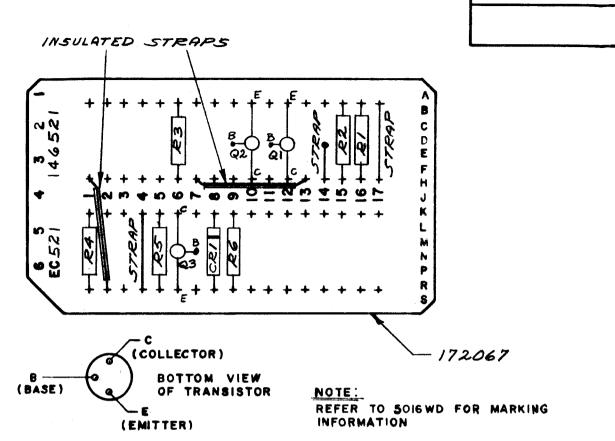
APPROVALS

E OF M N

CORPORATION

146520

ET-04147 TC255-6-541



REF. Design	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
CR1	177108	1	Diode, D-2	Clamp
RI	129851	2	Resistor, Fixed 3300 .5W	Input Base
R2	118180	1	Resistor, Fixed 10K .5"	Bias
R3 R4	137442	1-1-	Resistor, Fixed 1500 .5W	Load
R5	118186	2	Resistor, Fixed 5600 .5W	Bias
R6		}	Same as R5	Load
01	177105	2	Transistor P-22	Amplifier
02 03	177224	1-1-	Transistor 2N398 A	Power
			Same as Ql	
EC	172067		Circuit Card, Etched	
		1-2-	Strap 24 AWG Bare Strap 24 AWG Insulated	
	<u> </u>	2	Strap 24 AWG Insulated	
	144495	3	PAD TRANSISTOR	
		 		
		ļ		All and a second
		1		
				

₹7.09(47 \$0255(6-54)

RELAY DRIVER &

EC 521

This card consists of one Relay Driver Circuit and one Receiving Input Amplifier. The Relay Driver consists of all and all with all not to be loaded greater than 30 volts or 100 ma. The circuit will operate with inputs of +8 and Gnd. With +8 volts applied at input (F) all is biased "OFF" and -6 volts appears on the base of all turning it "ON", thereby, energizing the relay. With Gnd applied at input (F), all is biased "ON" driving all to cutoff by applying +1.5 volts to the base of all with Q2 off, the relay is not operated.

SYMBOLS

RELAY
DRIVER

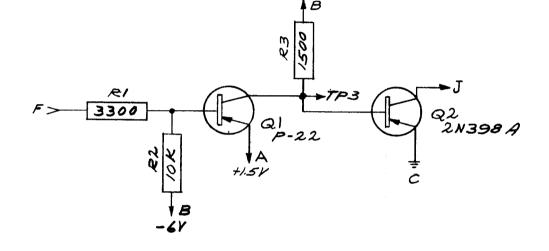
N 5/R

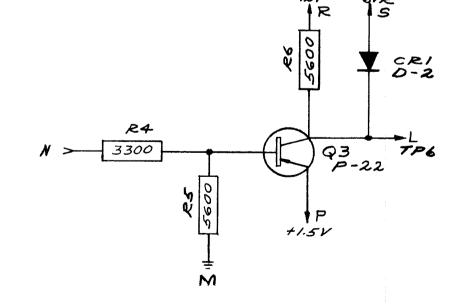
CIRCUIT BOARD EC 521

SSUE DATE AUTHINO.

146521

The Receiving Input Amplifier is used to convert a \pm 8 volts signal into a zero, -6 volt output. With +8 at input (N), Q3 is biased "OFF" making output (L) a -6 volt. With -8 volts at input (N) Q3 is biased "ON" placing output (L) at approximately \pm .75 volts or ground.





5 TRAP

A +1.5 Y

B -6 Y

GND.

M GND.

P +1.5 Y

R -12 Y

5 -6 R

APPROVALS

O AND R E OF M

D E-MUMBER

PROD. NO. 146521

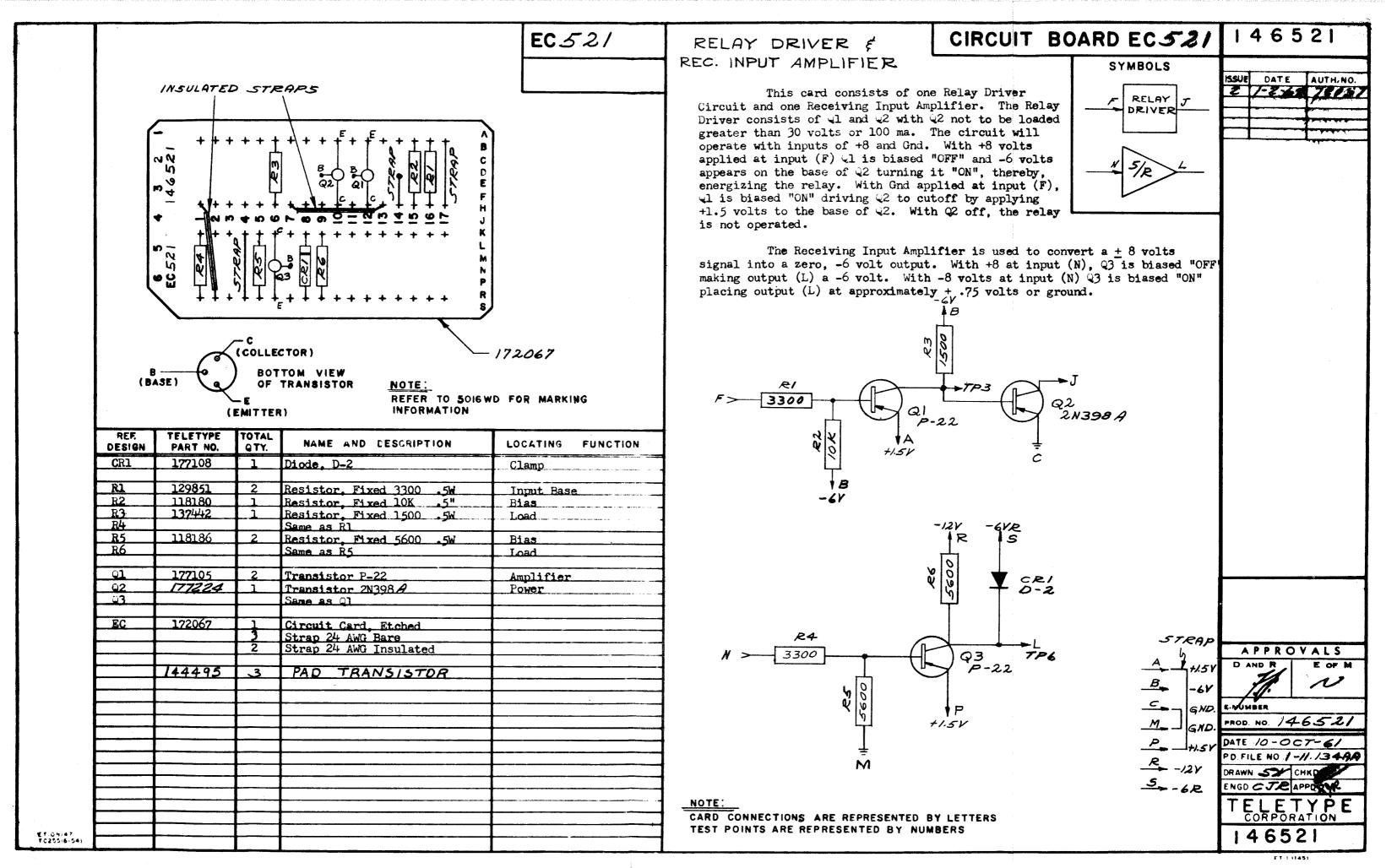
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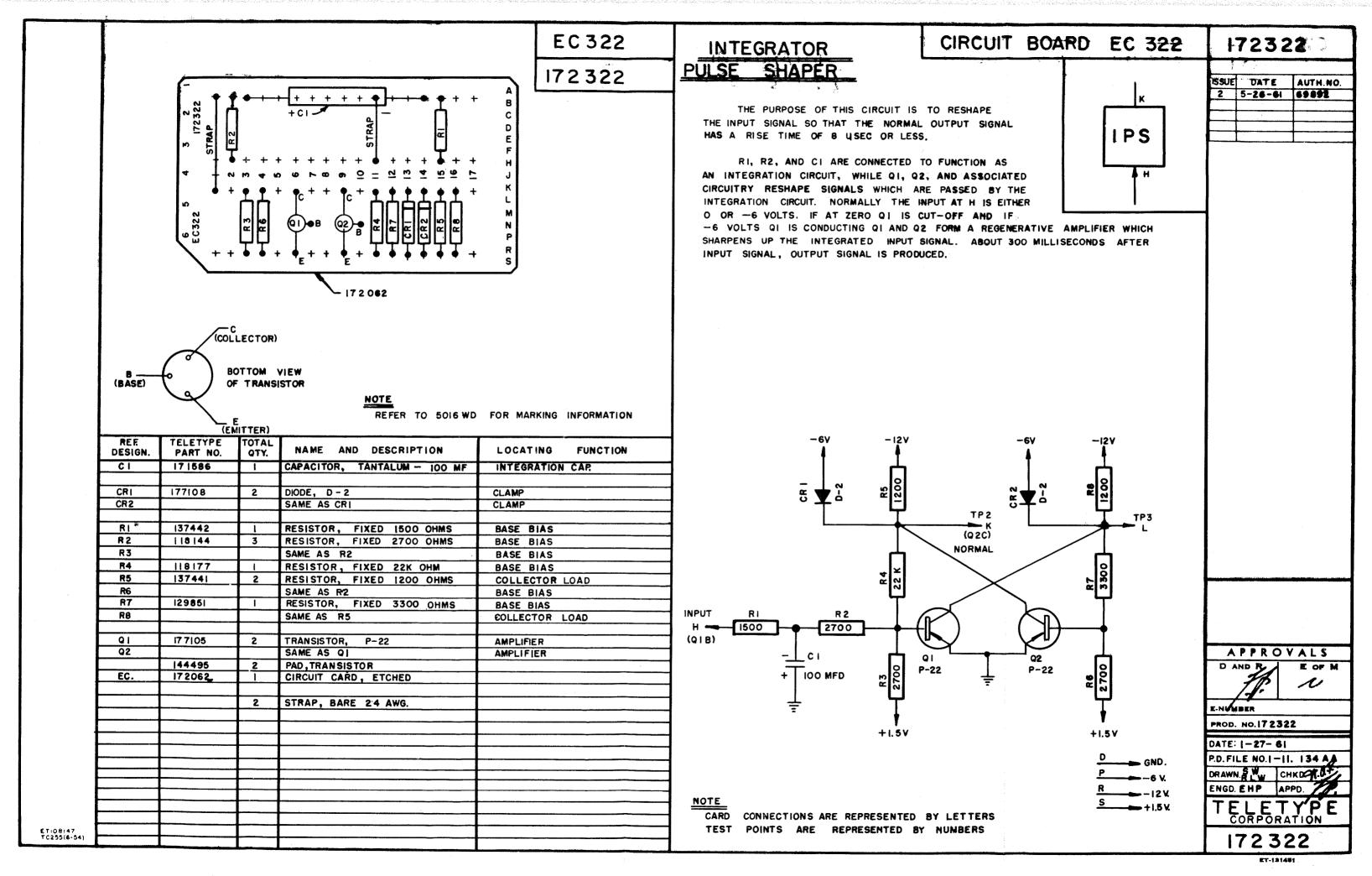
DRAWN SW CHKD

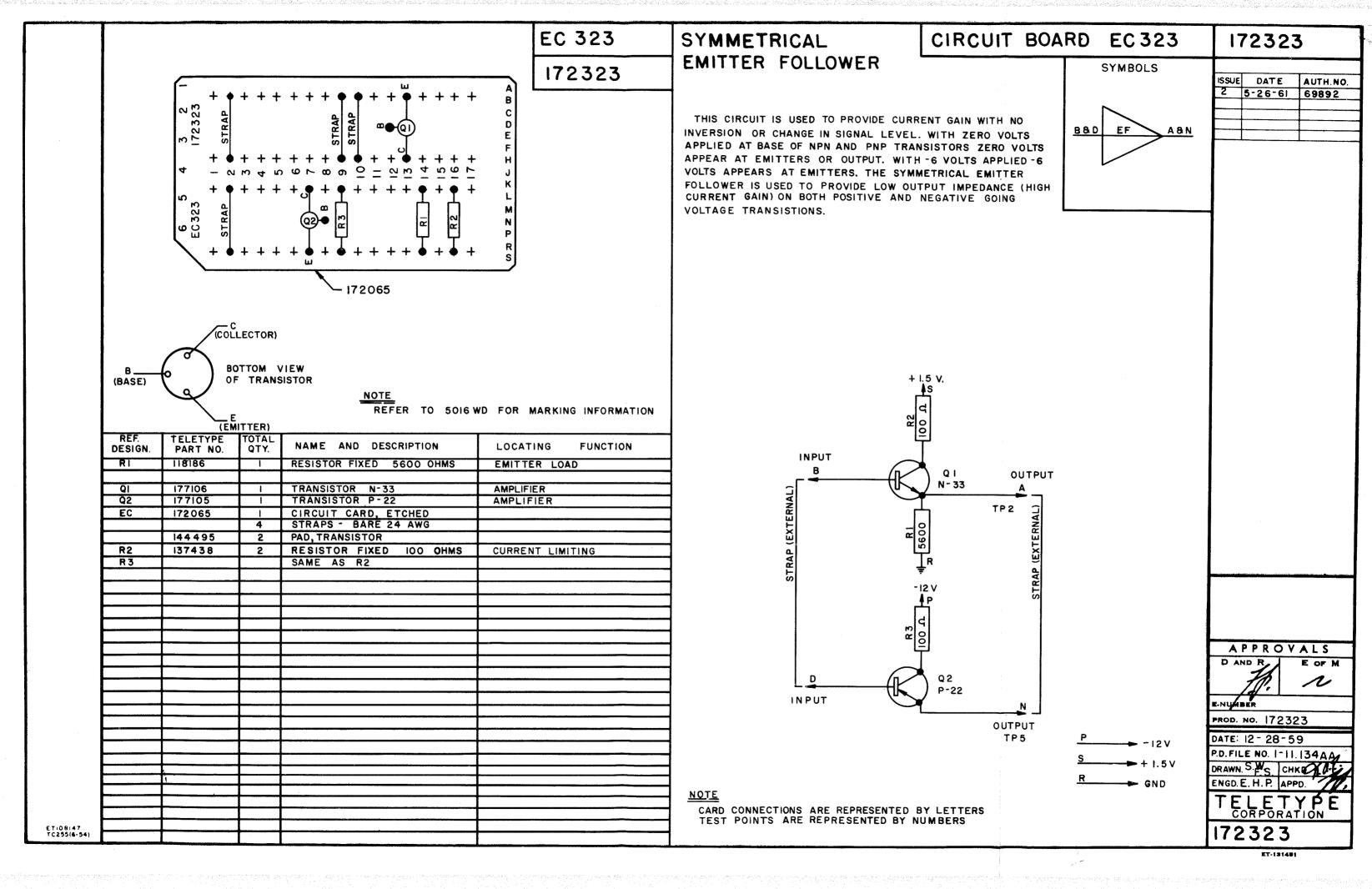
TELETYPE CORPORATION 146521

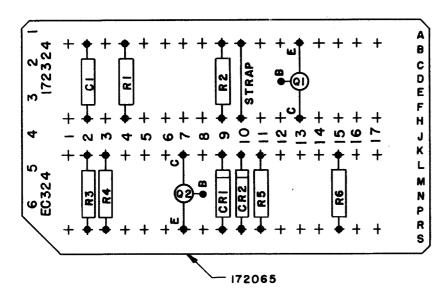
NOTE:

CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS









EC324

172324

INVERTER AND PULSE **AMPLIFIER**

CIRCUIT BOARD EC324

SYMBOLS

172324

ISSUE DATE AUTH.NO. 2 5-26-61 69892 3 8-2-61 70507 4 10.16.61 71626

APPROVALS

E of M

1

D AND R

NUMBER

THIS CARD CONSISTS OF A PNP COMMON EMITTER INVERTER AMPLIFIER AND A PULSE AMPLIFIER

QI IS REVERSE BIAS AT APPROXIMATELY 1.5 VOLTS AND THE COLLECTOR IS CLAMPED TO -6V. WITH -6 VOLTS APPLIED AT TERMINAL B, QI IS DRIVEN INTO SATURATION CAUSING THE COLLECTOR POTENTIAL TO RISE (-6V TO CV) FOR DURATION OF THE INPUT SIGNAL.

PULSE AMPLIFIER

Q2 IS REVERSED BIAS AT APPROXIMATELY +1.5V WHICH HOLDS Q2 OFF, WITH A NEGATIVE GOING 6V (OV TO-6V) TRANSISTION APPLIED TO DIFFERENTIATING CAPACITOR CAUSING BASE POTENTIAL TO GO NEGATIVE FOR A SHORT DURATION OF TIME. THIS CAUSES 92 TO CONDUCT AND THE COLLECTOR POTENTIAL IS AT O VOLTS DURING THIS TIME.

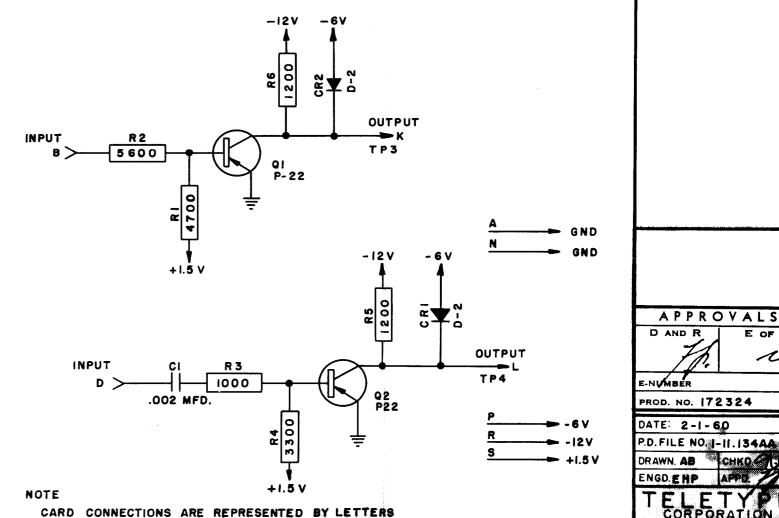
	(COL	LECTOR)	
B ——(BASE)	OF	TTCM V TRANS	
REF	TELETYPE	TOTAL	
DESIGN	PART NO.	QTY.	NAME

ET108147 TC255(6-54)

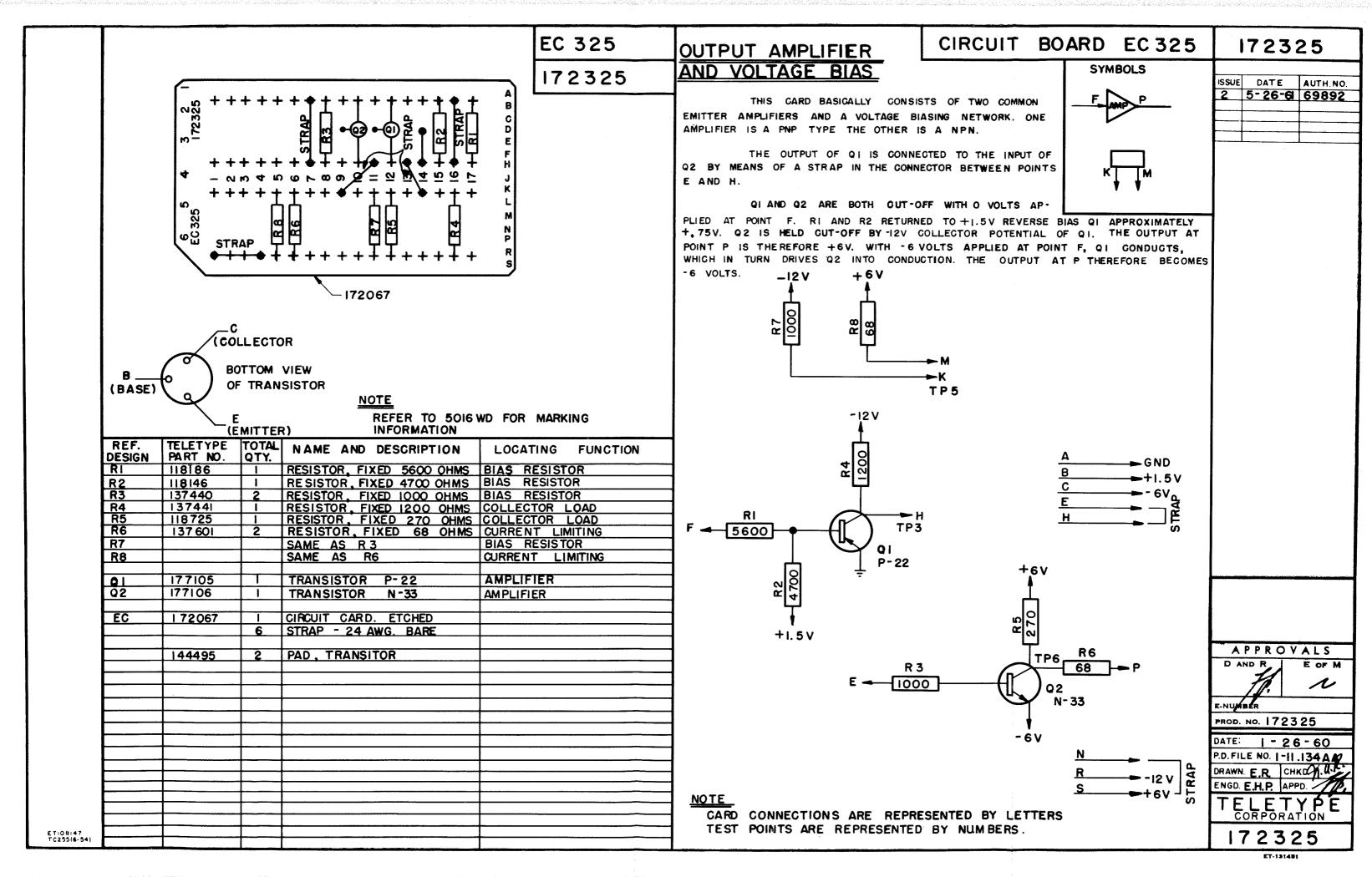
REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
CI	177332		CAPACITOR, CERAMIC .002 MFD	COUPLING
CRI	177108	2	DIODE D-2	CLAMP
CR2			SAME AS CRI	CLAMP
RI	118146	-	RESISTOR, FIXED 4700 OHMS	BIAS
R2	118186	1	RESISTOR, FIXED 5600 OHMS	BIAS
R3	137440	1	RESISTOR, FIXED 1000 OHMS	BIAS
R4	129851	1	RESISTOR, FIXED 3300 OHMS	BIAS
R5	137441	2	RESISTOR, FIXED 1200 OHMS	COLLECTOR LOAD
R6			SAME AS R5	COLLECTOR LOAD
91	177105	2	TRANSISTOR P-22	AMPLIFIER
Q2			SAME AS QI	AMPLIFIER
EC	172065	ı	CIRCUIT CARD, ETCHED	
		ı	STRAP BARE 24 AWG	
	1444 95	2	PAD, TRANSISTOR	
		+	,	

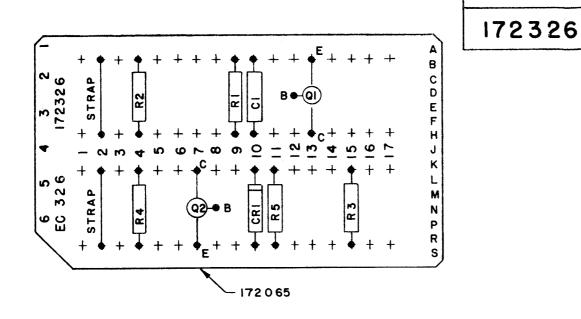
NOTE

REFER TO 5016 WD FOR MARKING INFORMATION



TEST POINTS ARE REPRESENTED BY NUMBERS





COLLECTOR)

(EMITTER)

(BASE)

ET:08:47 TC255(6-54) BOTTOM VIEW OF TRANSISTOR

NOTE

REFER TO 5016 WD FOR MARKING INFORMATION

EC 326

TELETYPE TOTAL REF. FUNCTION NAME AND DESCRIPTION LOCATING PART NO. DESIGN. CAPACITOR, CERAMIC .002 MFD COUPLING CAP 1793332 C1 CLAMPING DIODE 177108 DIODE, D-2 CR1 RESISTOR, FIXED 1000 OHMS BASE BIAS 137440 R1 RESISTOR, FIXED 3300 OHMS BASE BIAS 129851 R2 COLLECTOR LOAD RESISTOR, FIXED 1200 OHMS 137441 R3 EMITTER LOAD RESISTOR, FIXED 5600 OHMS 118186 R4 CURRENT LIMITING RESISTOR, FIXED 100 OHMS 137438 R5 1 AMPLIFIER TRANSISTOR, P-22 01 177105 AMPLIFIER SAME AS Q1 Q2 CIRCUIT CARD, ETCHED 1 EC 172065 STRAPS BARE 24AWG 2 PAD, TRANSISTORS 144495

PULSE AMP, AND EMITTER FOLLOWER (PNP) CIRCUIT BOARD EC326

SYMBOLS

172326

ISSUE DATE AUTH.NO.

2 5-26-6/ 69892

3 //-/6-6/ 7/626

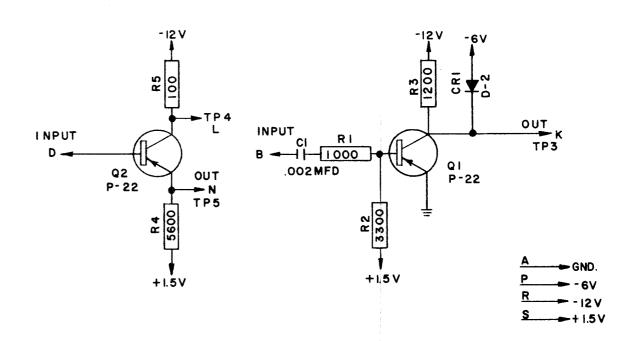
4 4-5-62 23031

PULSE AMP

Q1 IS REVERSED BIAS AT APPROXIMATELY +1.5V WHICH HOLDS Q1 OFF. WITH A NEGATIVE GOING 6V (OV TO -6V) TRANSISTOR APPLIED TO DIFFERENTIATING CAPACITOR CAUSING BASE POTENTIAL TO GO NEGATIVE FOR A SHORT DURATION OF TIME. THIS CAUSES Q2 TO CONDUCT AND THE COLLECTOR POTENTIAL IS AT O VOLTS DURING THIS TIME.

PNP EMITTER FOLLOWER

THIS CIRCUIT IS A EMITTER FOLLOWER USED TO PROVIDE CURRENT GAINS WITH NO INVERSION OR CHANGE IN THE SIGNAL LEVEL. WITH ZERO VOLTS APPLIED AT THE BASE, ZERO VOLTS APPEARS AT EMITTER. THE PNP EMITTER FOLLOWER IS USED TO PROVIDE LOW OUTPUT IMPEDANCE (HIGH CURRENT GAIN) ON THE NEGATIVE GOING VOLTAGE TRANSITION (-6 TO 0 VOLTS).



NOTE

CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

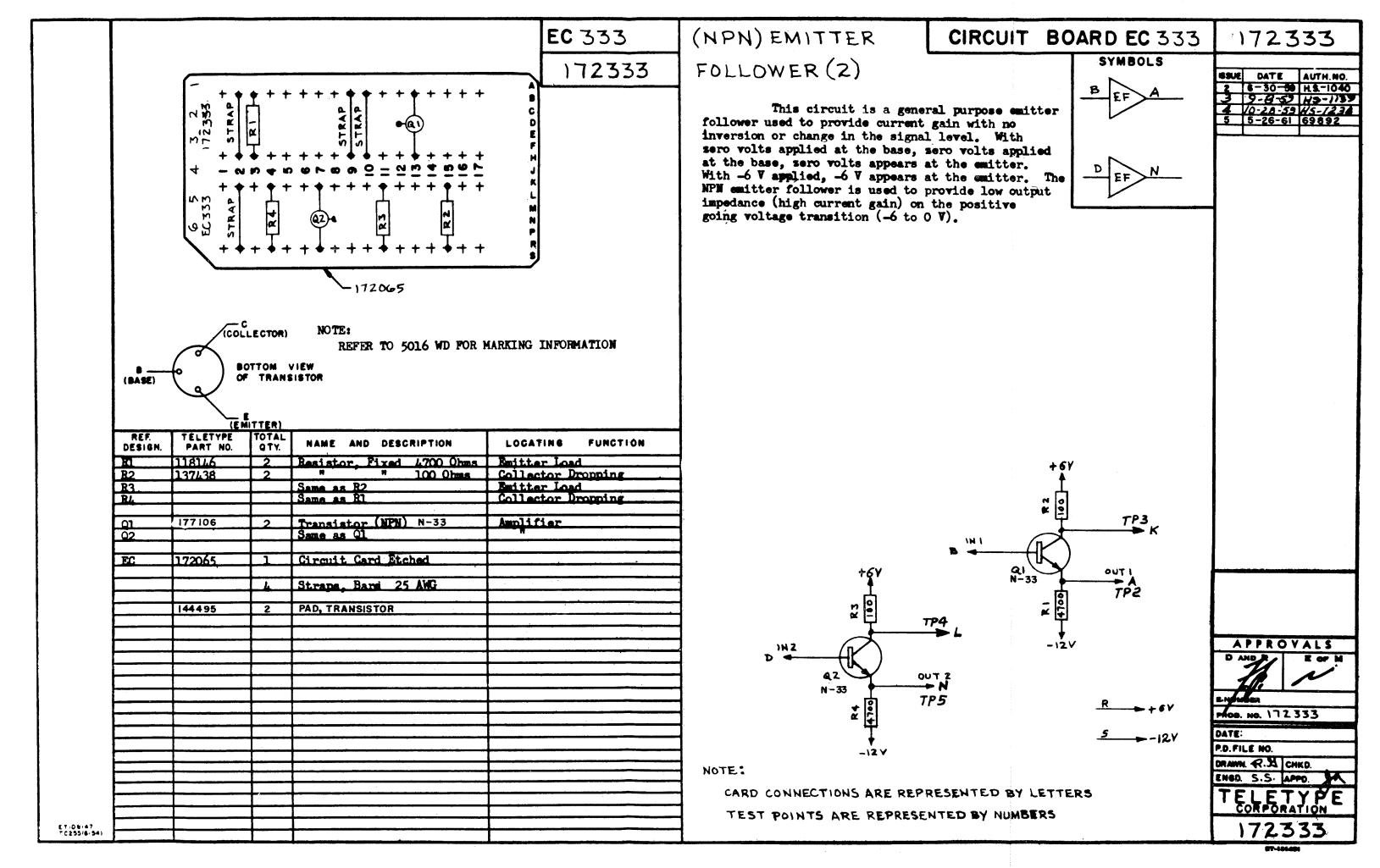
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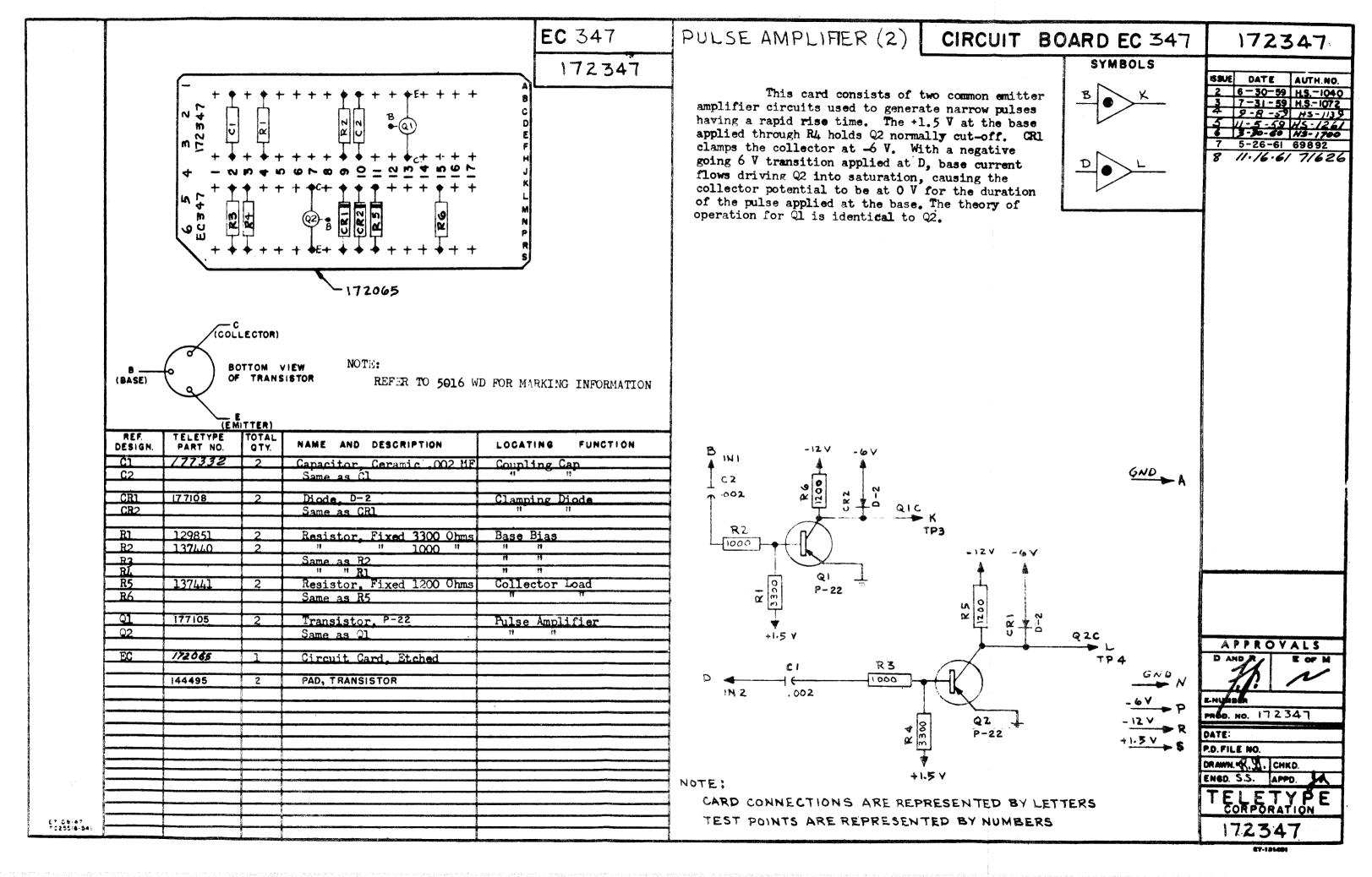
PROD. NO. 172326

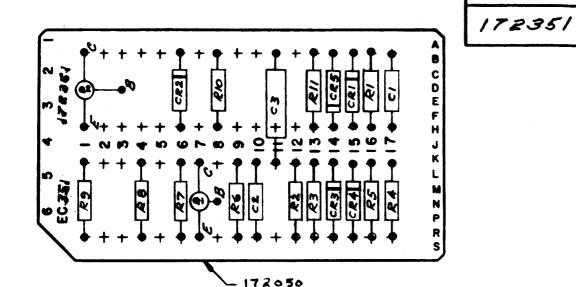
DATE: 2- 19-60 P.D.FILE NO. (-1), 134 AA

DRAWN. S.W. E.S. CHKD.

TELETYPI CORPORATION







B BOTTOM VIEW OF TRANSISTOR

_ E (EMITTER) TELETYPE TOTAL NAME AND DESCRIPTION LOCATING FUNCTION DESIGN. PART NO. 177332 Coupling Capacitor, Caramic .002MFD <u>C2</u> 177331 Capacitor, Ceramic .001MFD Feedback .C3 Capacitor Mylar .25M50 Delay ITIBET 177108 Diode 0-2 . CRI Gate CR2 Coupling CR3 Same as CRI Clamp Same as CRI Clamo CR5 Same as CRI Gate RI Resistor, Fixed 22K Ohms 118177 Bias R2 137442 Resistor, Fixed 1500 Chms Pias Resistor, Fixed 10K Ohms R3 118180 Bias Collector Load 137441 Resistor, Fixed 1200 OHms PL R5 Collector Load Same as R4 129851 118144 Resistor, Fixed 3300 Ohms Resistor, Fixed 2700 Ohms Feedback Pias R8 Same as R3 Bias R9 143656 Resistor, Fixed 51 Ohms Common Emitter R10 118147 Resistor, Fixed 6800 Ohms Fias Rll Resistor, Fixed 3900 Ohms Pias 77105 Amplifier Transistor, P-22 Same as Q1 17203 Circuit Card, Etched 144495 PAD, TRANSISTOR

VARIABLE PULSE

EC 351

REFER TO 5016 WD FOR MARKING INFORMATION

DELAY

(.4/ TO 63MS)

The purpose of this circuit is to generate a signal of variable width as determined by the input signal applied at point A.

tias current through k10 and R2 in parallel with CR5, R3 and R8. The collector of C2 is approximately at 0 volts and Q1.collector is at -6V Q1 is maintained in cut-off state by cross coupling resistor R6 and R7 and returning to +1.5 volts holding base potential at approximately +1 volt.

Capacitor C1, R1 and CR1 combine to form gate where by when -6V is applied to E and a 6 volt positive pulse applied to Terminal C will fail to trigger circuit, however, if Terminal E is at 0 volts a positive pulse will turn -2 off and remain cut-off until C3 can discharge to a level through R3 and K11 to permit -2 to conduct.

The aiming potential is varied by applying 0 or -6 volts on Terminal A since Rll is part of discharge path thus increasing or decreasing time out of the circuit. With -6 volts at A time out is approximately . #/ milliseconds. With 0 volts applied the time out is approximately //3 milliseconds.



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15 SUE	DATE	AUTH NO.
5	5-26 6l	69892
6	11.16.61	71626
1	2-6-64	80254
		T

MAGE

	NOR OUT TP3	120	-6V	R3 R84	INVER OUT!	82 X 400 X 100 X 1	/0 K3		
C2) .001MFD	3300	Q1 P-22		CR2 D-2 -P-22) X 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	CRS C3	25 MFP. D-2 CRI	BIAS IN	
NOTE	2700		+1.5 >			R8 10K	ā [v .v

CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

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PROD. NO. / 72351

DATE: 7-DEC-57

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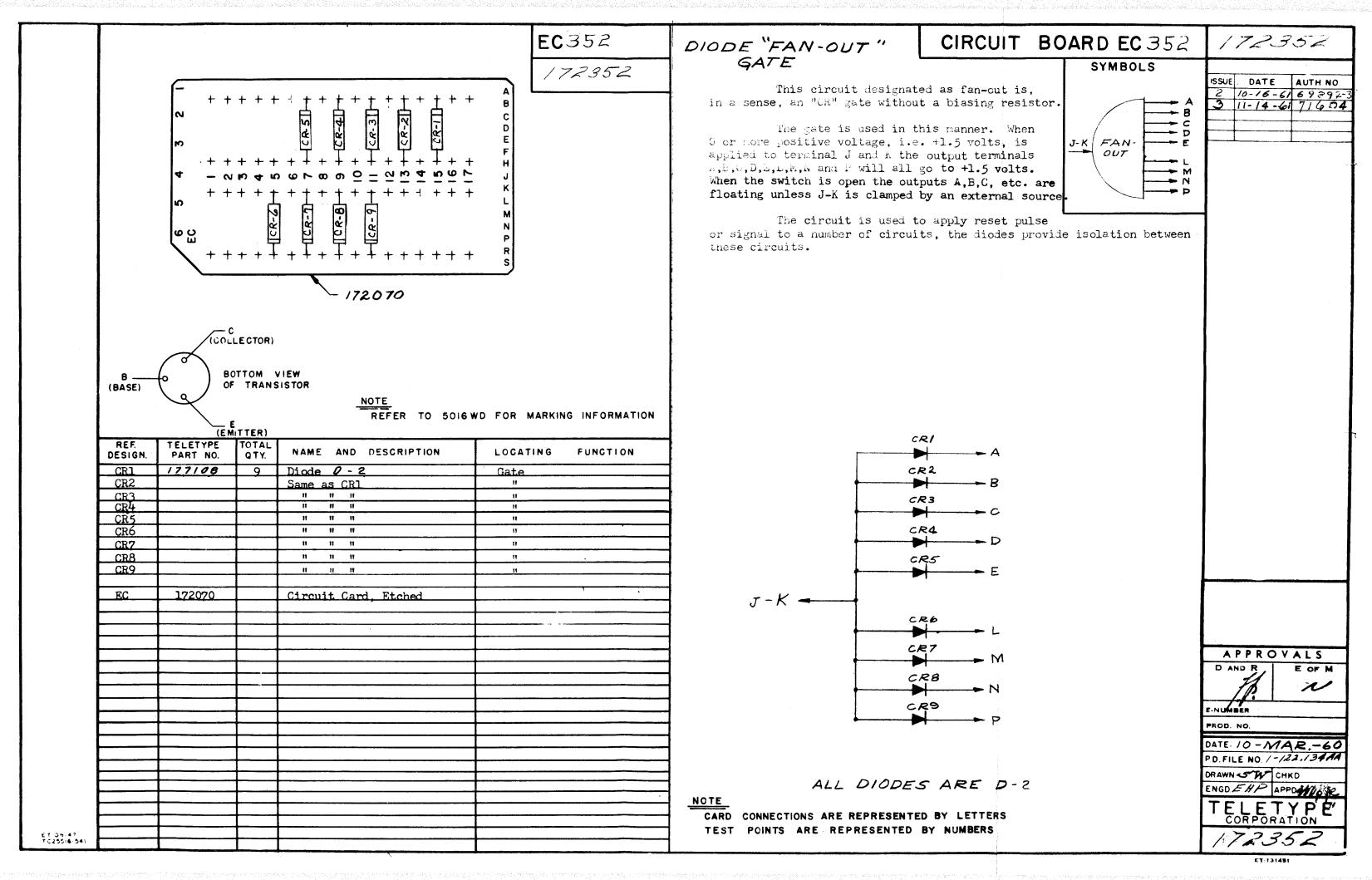
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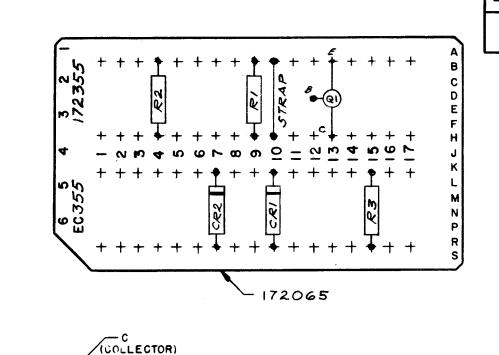
TELETYPE

72351

ET 34:47 TC255(6:54)

ET I MARA





BOTTOM VIEW OF TRANSISTOR NOTE REFER TO 5016 WD FOR MARKING INFORMATION __ E (EMITTER)

(BASE)

ET 38:47 TC255(6-54)

TELETYPE PART NO. REF TOTAL NAME AND DESCRIPTION LOCATING FUNCTION QTY. DESIGN. R.L 129851 Base Bias Resistor, Fixed 3300 Ohms Resistor, Fixed 5600 Ohms Same as R2 Base Bias Collector Load R2 118186 R3 CRI Diode D-2 Clamping 177108 Gate Same as CR1 CR2 Transistor 2N398A Amplifier ्य 177224 172065 Circuit Card. Etched Strap Bare 24 AWG PAD, TRANSISTOR 144495

RECEIVER INPUT

EC 355

172355

AMPLIFIER

CIRCUIT BOARD EC 355

172355

SYMBOLS

This card consist of a common emitter PNP amplifier used to convert a maximum DC signal of +50 to -50 volts and minimum signal of +3 to -3 volts to a -6 to +1.5 volt signal.

With a maximum of +50 volts and minimum of +3 volts on Terminal B, Ql is cut off and Terminal K is at -6 volts. With a maximum of -50 volts and minimum of -3 volts on Terminal B, Q1 conducts and the output is at approximately +1.5 volts.

Diode CR2 provides an "OR" gate. When Terminal N is at 0 volts, the diode is forward bias and 0 volts appears at K when Ql is cut off.

ISSUE DATE AUTH NO. 2 5-26-61 69892

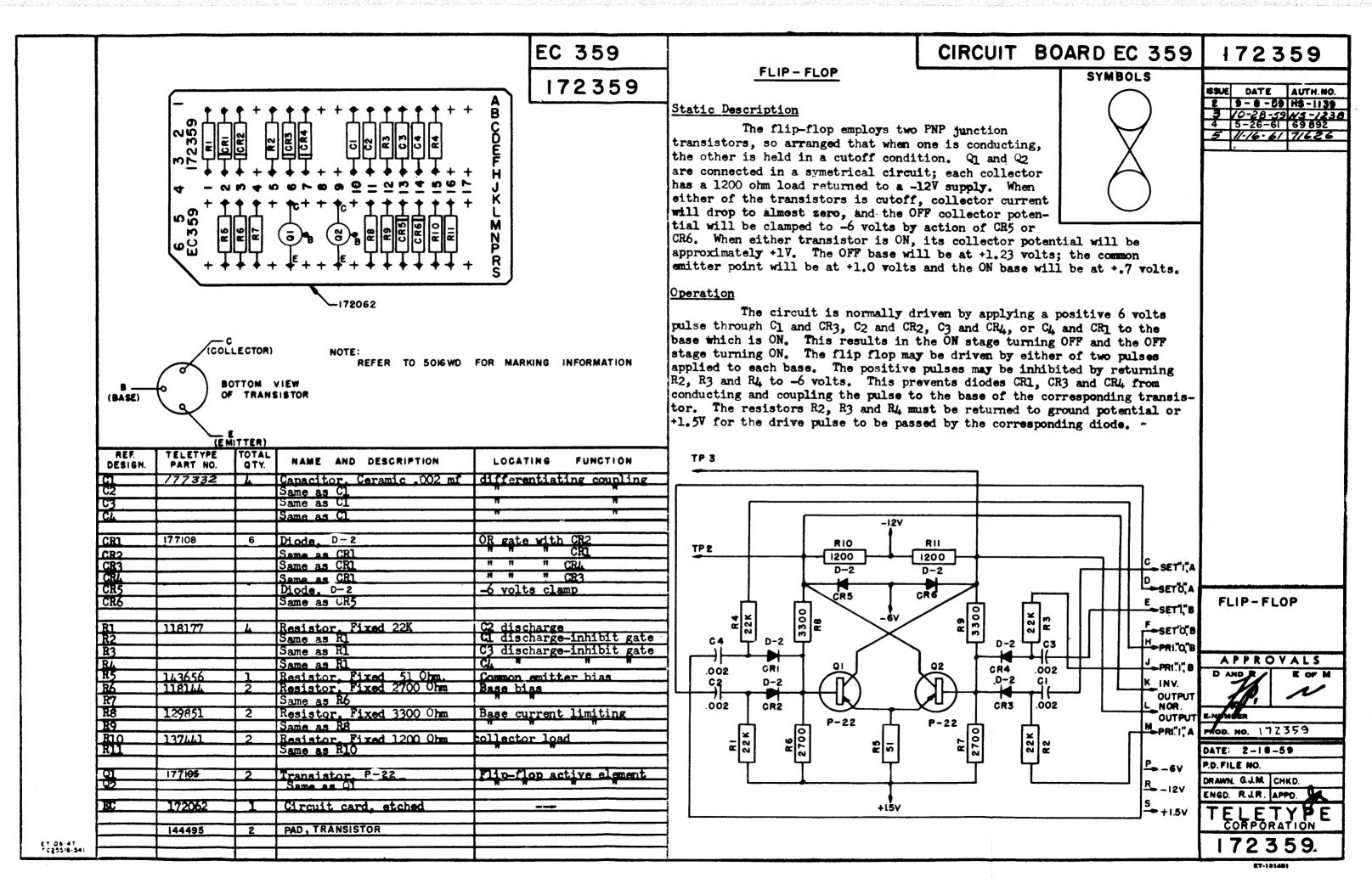
-12VOUT INPUT TP3 3300 QI 2N398A RZ +1.5Y TP5 STRAP

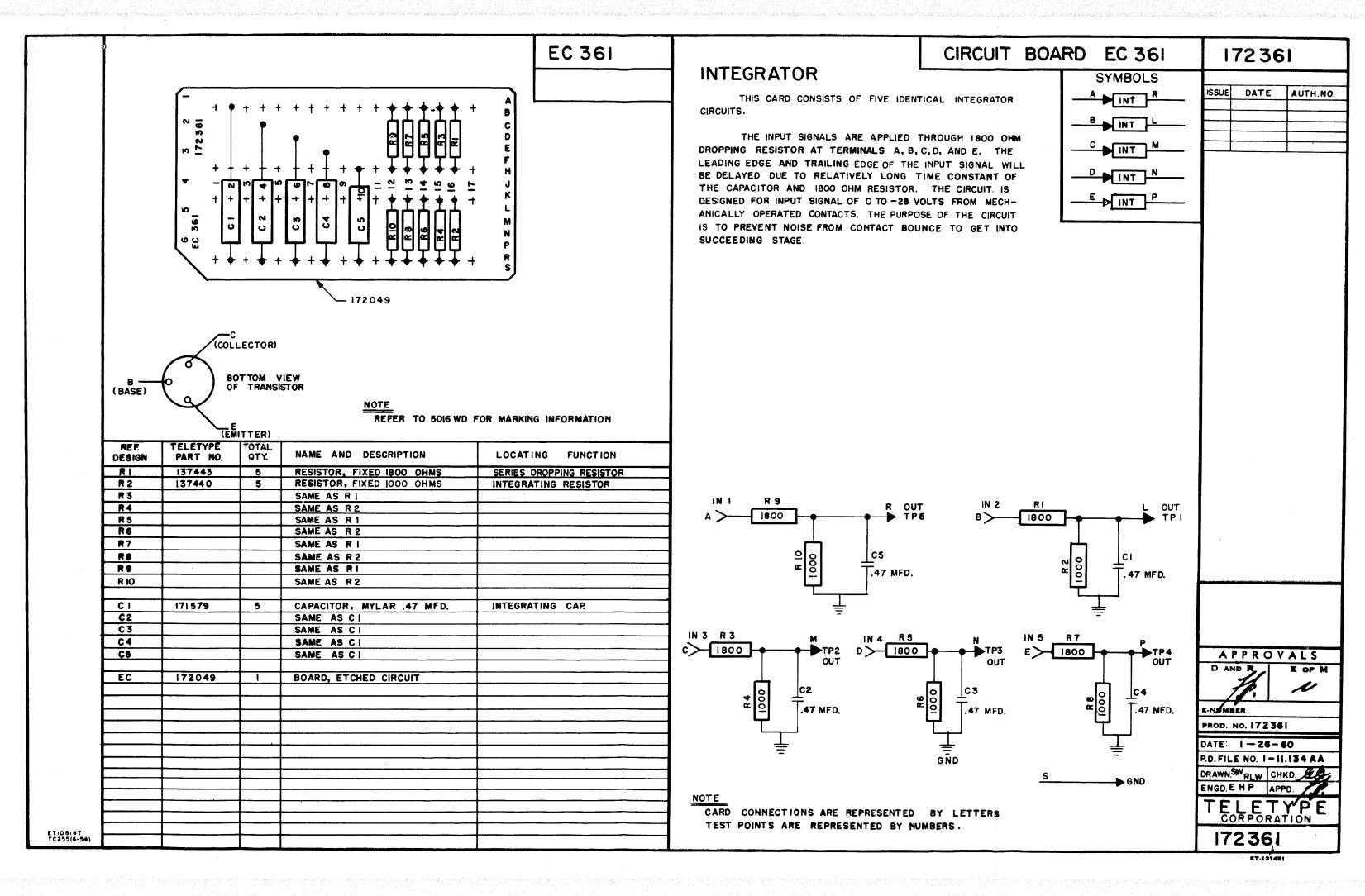
NOTE

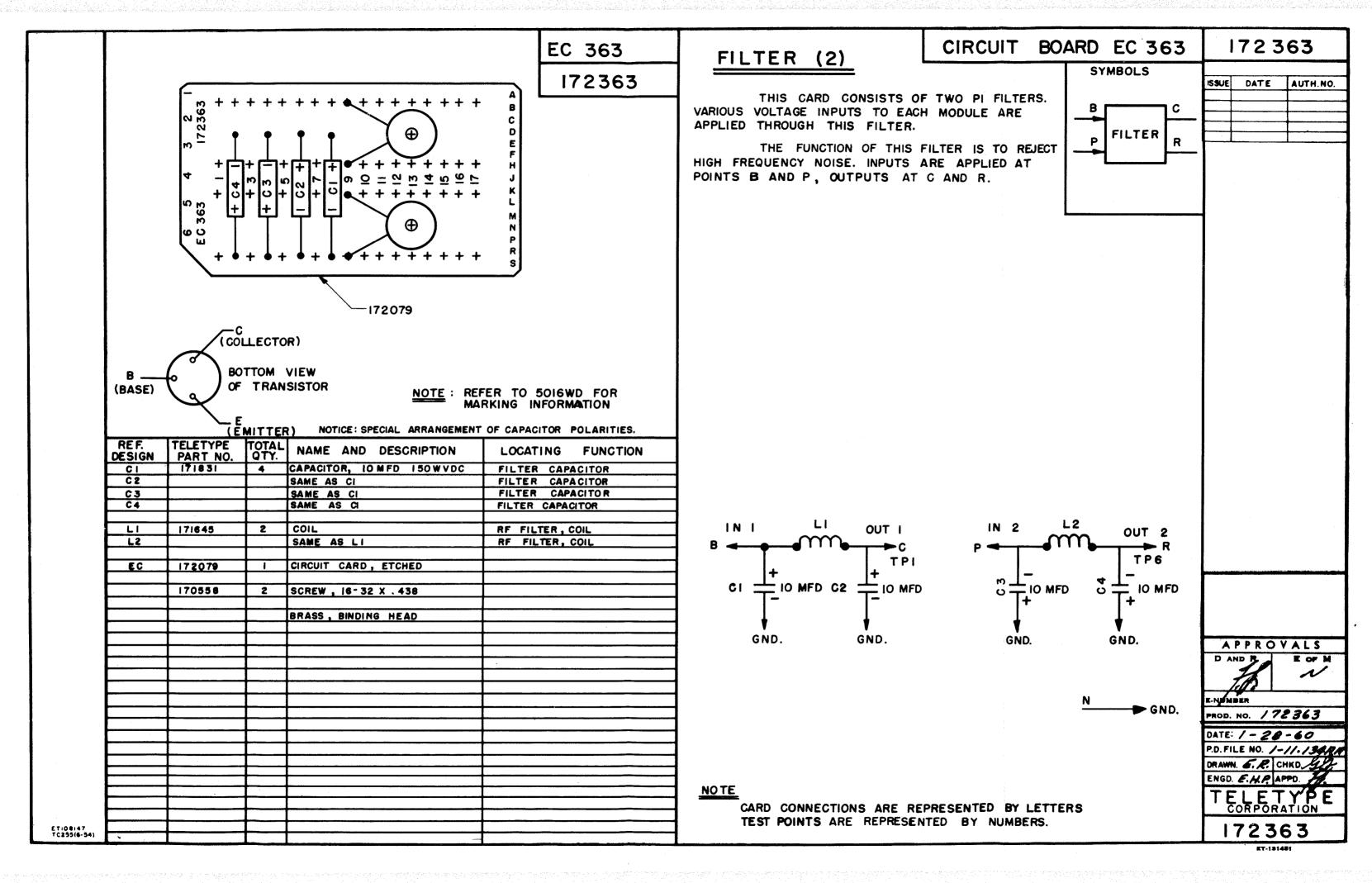
CARD CONNECTIONS ARE REPRESENTED BY LETTERS TEST POINTS ARE REPRESENTED BY NUMBERS

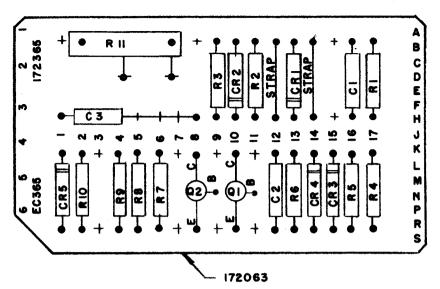
APPROVALS D AND R E OF M -NUMBER FROD. NO. 172355 DATE: 26 - JAN - 60 P.D. FILE NO. 1-11.134A

DRAWN S WE CHKD Z ENGO ENP APPON









NOTE

NAME AND DESCRIPTION

CAPACITOR, CERAMIC .002 MF

CAPACITOR, CERAMIC .001 MF

CAPACITOR, MYLAR .25 MFD

RESISTOR, FIXED 22K OHMS

RESISTOR, FIXED 1500 OHMS

RESISTOR, FIXED 3900 OHMS

RESISTOR, FIXED 1200 OHMS

RESISTOR, FIXED 3300 OHMS

RESISTOR, FIXED 2700 OHMS

RESISTOR, FIXED 10K OHMS

RESISTOR, FIXED 6800 OHMS

RESISTOR, VARIABLE 10K OHMS

RESISTOR, FIXED 51 OHMS

TRANSISTOR, P-22

CIRCUIT CARD, ETCHED

SCREW, 2-56 x .431, FIL.

STRAP 24 AWG BARE

NUT, 2-56, HEX.

PAD, TRANSISTOR

DIODE, D-2

DIODE, D-2

SAME AS CR2

SAME AS CR2

SAME AS CR2

SAME AS R4

SAME AS Q1

REFER TO 5016 WD FOR MARKING INFORMATION

LOCATING

COUPLING

FEEDBACK

COUPLING

TIMING

GATE

CLAMP

CLAMP

GATE

GATE

BIAS

BIAS

BIAS

TIMING

SWITCH

SWITCH

TIMING

FEEDBACK

COLLECTOR LOAD

COLLECTOR LOAD

(COLLECTOR)

__ E (EMITTER)

TOTAL

QTY.

5

2

2

2

2

TELETYPE

PART NO.

177332

177331

171587

177108

118177

137442

143667

137441

129851

118144

118180

143656

118147

171565

177105

172063

110446

144495

1178

BOTTOM VIEW

OF TRANSISTOR

EC 365 172365 VARIABLE ONE SHOT

CIRCUIT BOARD EC365 172365

SYMBOLS

ISSUE DATE AUTH.NO. 2 5-26-61 69892 11.16.61 71626

.65 TO 2.2 MS

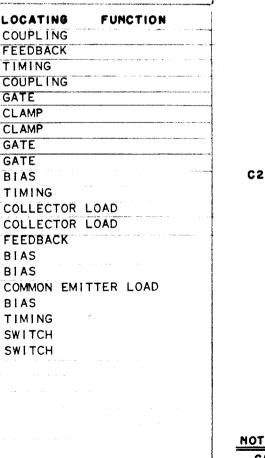
THE PURPOSE OF THIS CIRCUIT IS TO GENERATE A PULSE OF KNOWN WIDTH IN THE RANGE OF .65 MILLISECONDS TO 2.2 MILLISECONDS IN RESPONSE TO AN INPUT. NORMAL (POSITIVE GOING) AND INVERTED OUTPUTS ARE PROVIDED.

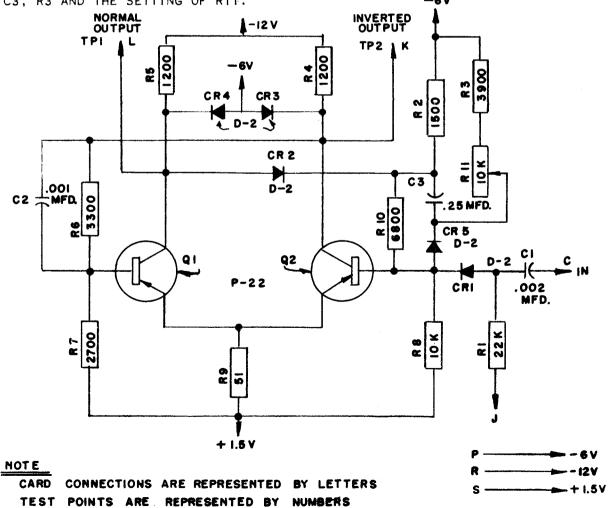
THE QUIESCENT STATE OF THIS CIRCUIT IS THAT Q2 IS SATURATED, RECEIVING ITS BIAS CURRENT PRIMARILY THROUGH R2 AND R10 CONNECTED IN PARALLEL WITH CR5. R3 AND R11 TO -6V. THE COLLECTOR OF Q2 IS APPROXIMATELY AT ZERO VOLTS AND THE COLLECTOR OF 01 IS -6V. 01 IS MAINTAINED CUT-OFF BY CROSS COUPLING RESISTOR R6 AND RESISTOR R7 RETURNED TO +1.5V, HOLDING THE BASE

POTENTIAL OF Q1 AT APPROXIMATELY +1V. THE COMMON EMITTER POTENTIAL IS ZERO VOLTS SINCE Q2 IS SATURATED.

CAPACITOR C1, R1 AND CR1 COMBINE TO FORM AN INHIBIT GATE, WHEREBY WHEN -6V IS APPLIED AT POINT J, INPUTS RECEIVED AT POINT C WILL FAIL TO TRIGGER THE CIRCUIT. CONVERSELY THE CIRCUIT IS ENABLED WHEN POINT J IS RETURNED TO OV SINCE CRI WILL NOW PASS POSITIVE GOING TRANSITIONS.

THE CIRCUIT IS TRIGGERED AS FOLLOWS: A POSITIVE TRANSITION APPLIED AT POINT C DRIVES Q2 INTO CUT-OFF WHICH, IN TURN, ALLOWS Q1 TO CONDUCT. AS THE COLLECTOR OF Q1 APPROACHES OV, CR2 CONDUCTS CHARGING C3, AND MAINTAINING Q2 IN CUT-OFF. Q2 REMAINS CUT-OFF UNTIL C3 CAN DISCHARGE SUFFICIENTLY THROUGH VARIABLE RESISTOR R11 AND R3 TO PERMIT CONDUCTION OF Q2. THE PERIOD OF CONDUCTION OF Q1 IS PRIMARILY DETERMINED BY THE SIZE OF C3, R3 AND THE SETTING OF R11.





(BASE)

REF.

DESIGN

C1

C2

C3

CRI

CR2

CR3

CR4

CR5

R1

R2

R3

R4

R5

R6

R7

R8

R9

R10

R11

Q1

Q2

EC

APPD.

ELETYPE

CORPORATION

172365

APPROVALS

D AND R

PROD. NO.172365

DATE: 2-1-60

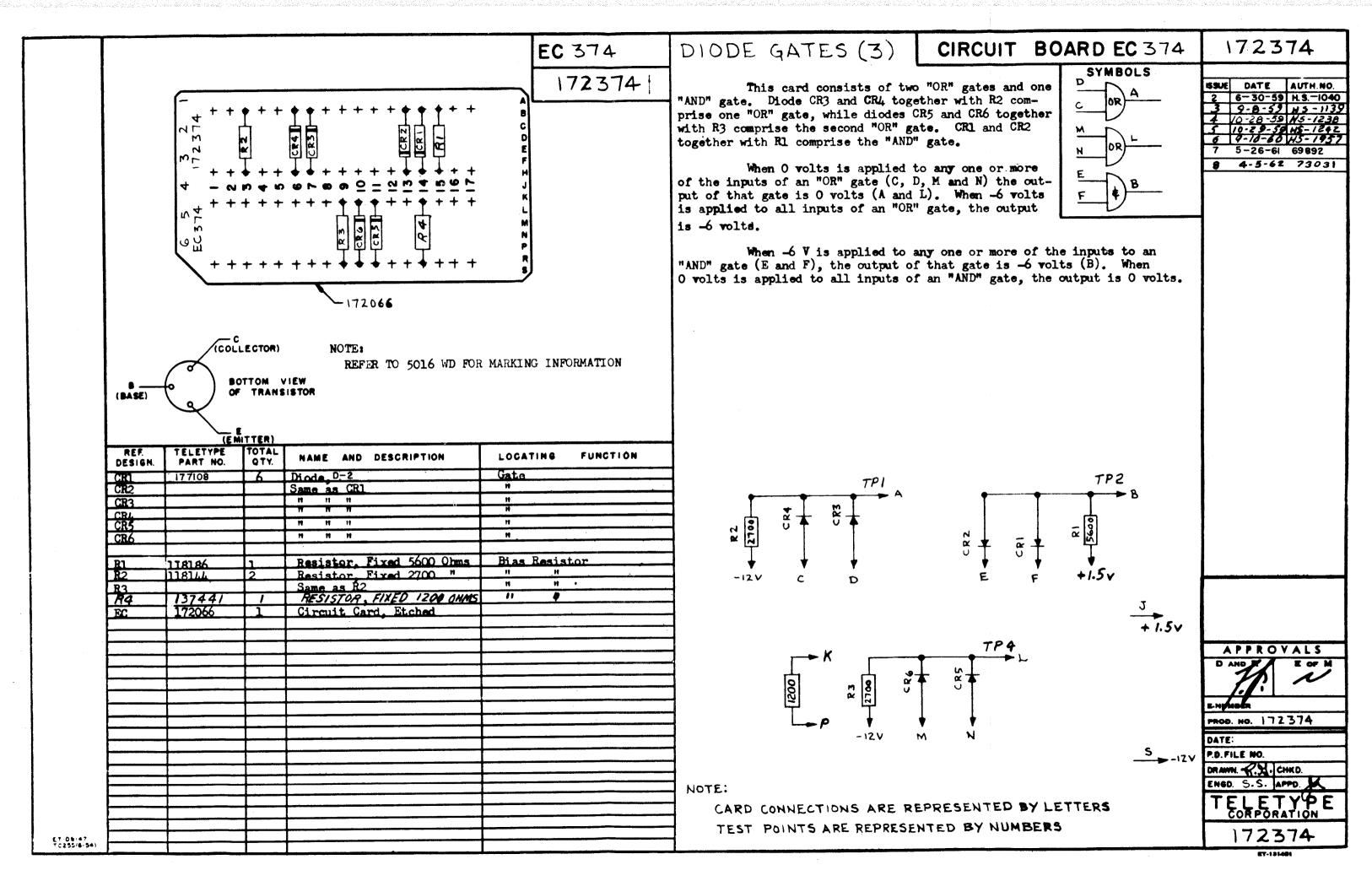
P.D. FILE NO. 1-11-134AA

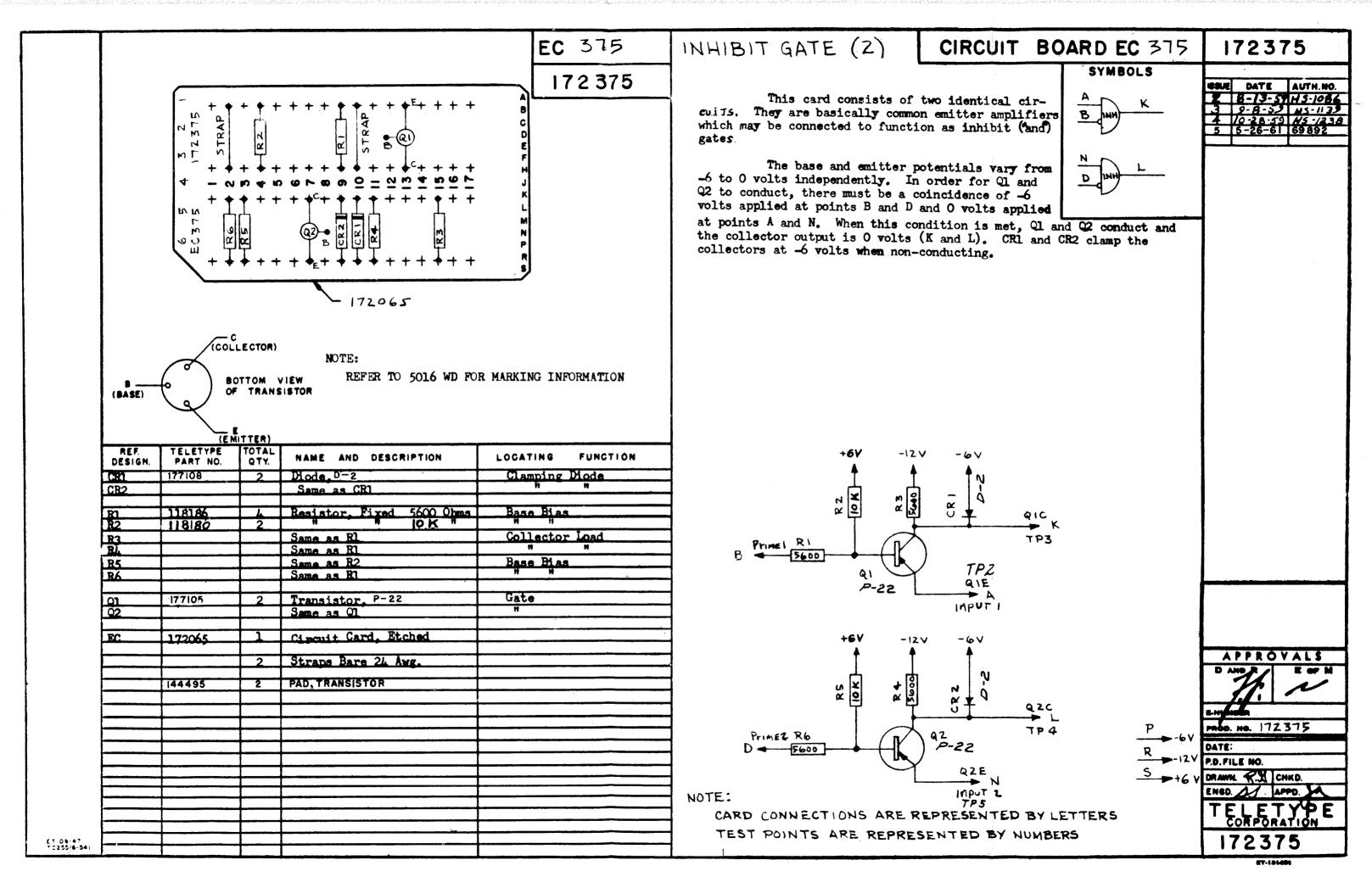
DRAWN. RLW CHKD. MIL

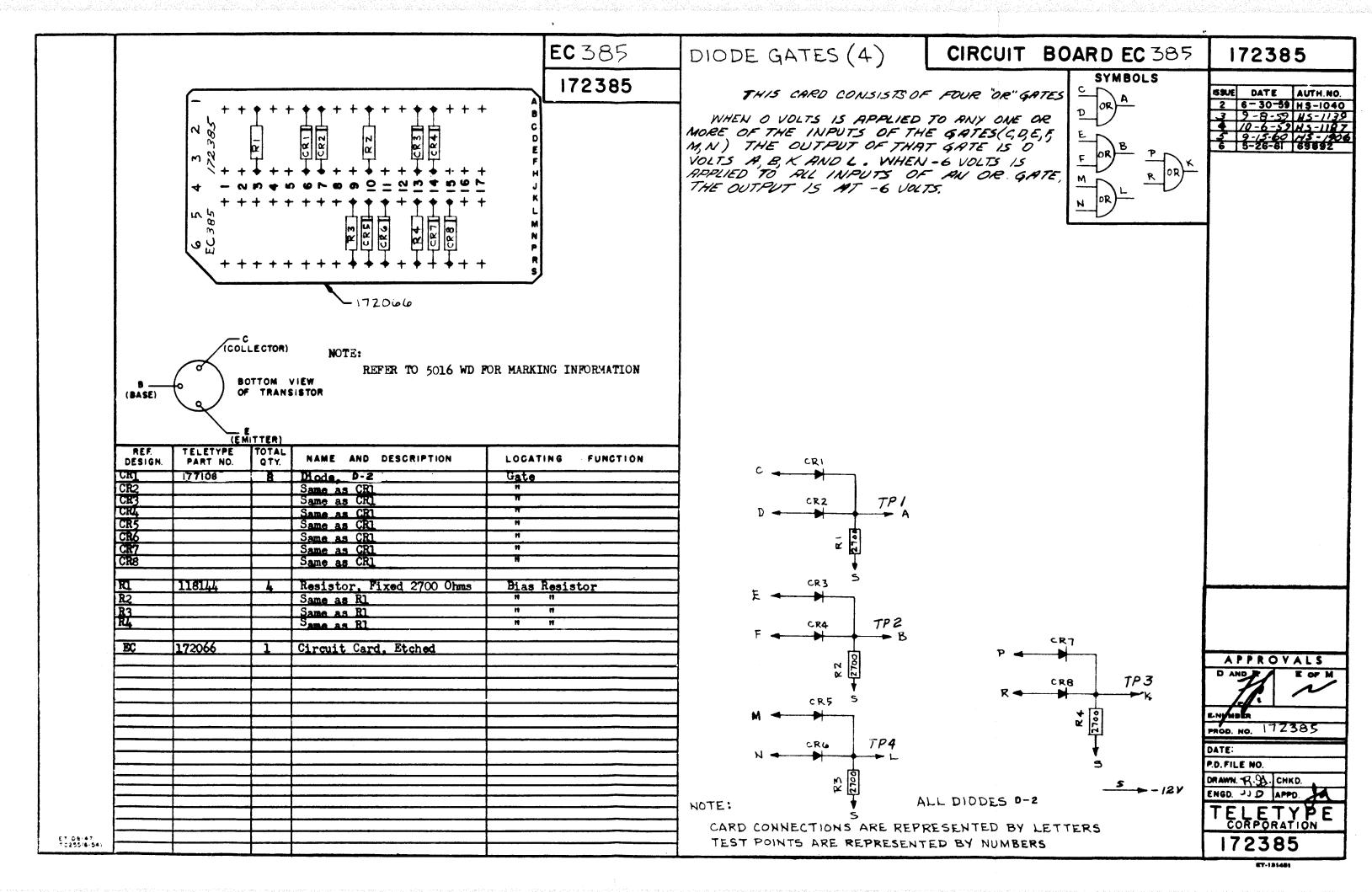
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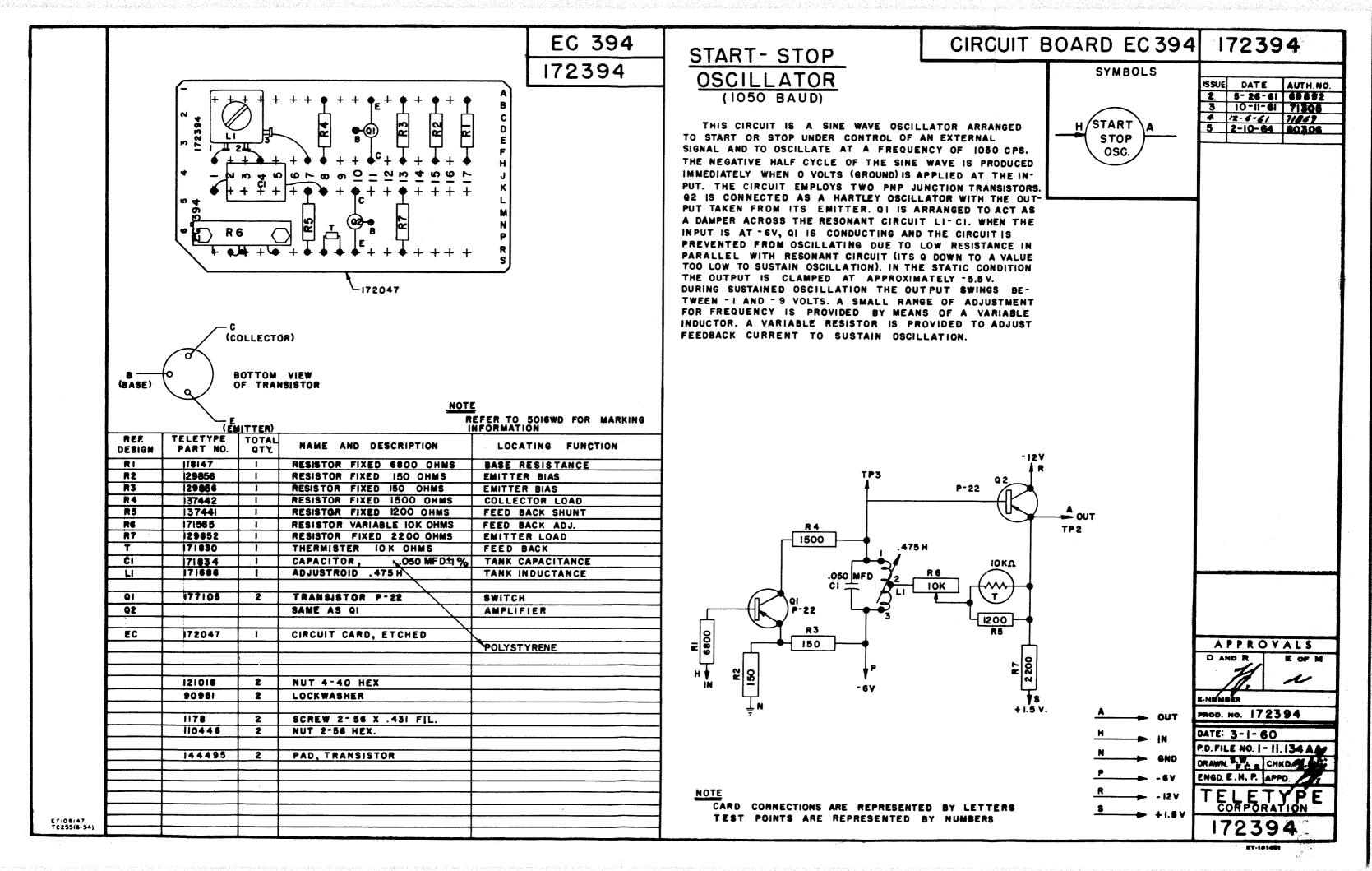
ENGD. EMP

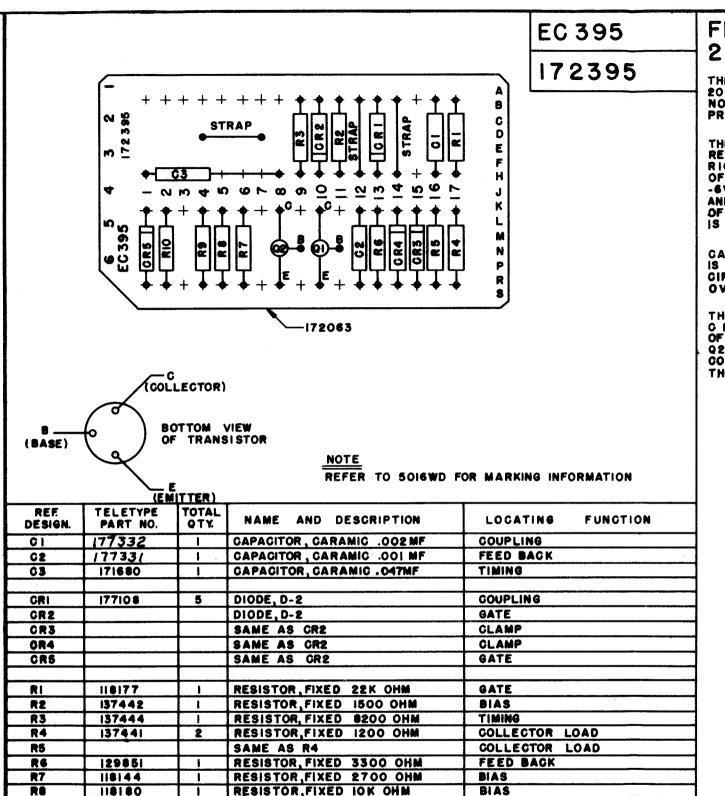
E OF M











RESISTOR, FIXED 51 OHM

GIRCUIT CARD, ETCHED STRAP 24 ANG BARE

TRANSISTOR, P-22

PAD. TRANSISTOR

SAME AS QI

RESISTOR, FIXED 6800 OHM

COMMON EMITTER LOAD

BIAS

SWITCH

SWITCH

143656

118147

177105

172063

144495

29 RIO

01

92

EC

ET:08:47 TC255(6-54)

FIXED ONE - SHOT 200 US

CIRCUIT BOARD EC 395

172395

SYMBOLS

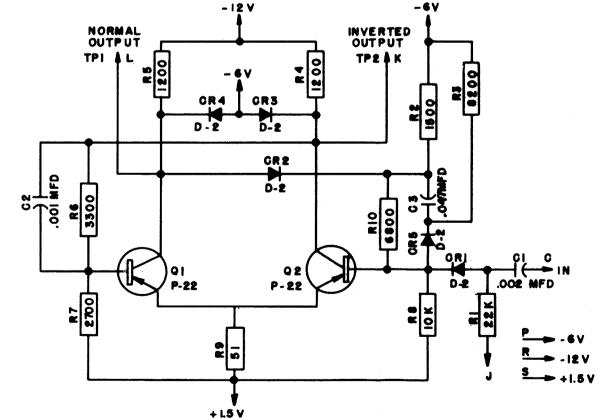
DATE AUTH.NO. 5-26-61 69692 3 /1·/6·6/ 7/626 4 1-15-64 80001

THE PURPOSE OF THIS CIRCUIT IS TO GENERATE A PULSE OF 200 MIGROSECONDS IN WIDTH IN RESPONSE TO AN INPUT. NORMAL (POSITIVE GOING) AND INVERTED OUTPUTS ARE

THE QUIESCENT STATE OF THIS CIRCUIT IS THAT Q2 IS SATURATED, RECEIVING ITS BIAS CURRENT PRIMARILY THROUGH R2 AND RIO CONNECTED IN PARALLEL WITH CR5, R3 TO -6V. THE COLLECTOR OF Q2 IS APPROXIMATELY OV AND THE COLLECTOR OF QI IS -6V. QI IS MAINTAINED CUT-OFF BY CROSS COUPLING OF RE AND R7 RETURNED TO + 1.5 V, HOLDING THE BASE POTENTIAL OF QI AT APPROXIMATELY + IV. THE COMMON EMITTER POTENTIAL IS OV SINGE Q2 IS SATURATED.

CAPACITOR CI, RI AND CRI COMBINE TO FORM AN INHIBIT GATE, WHEREBY WHEN - 6 V IS APPLIED AT POINT J, INPUTS RECEIVED AT POINT G WILL FAIL TO TRIGGER THE CIRCUIT. CONVERSELY THE CIRCUIT IS ENABLED WHEN POINT J IS RETURNED TO OV SINCE CRI WILL NOW PASS POSITIVE SOINS TRANSITIONS.

THE CIRCUIT IS TRIGGERED AS FOLLOWS: A POSITIVE TRANSITION APPLIED AT POINT C DRIVES Q2 INTO CUT-OFF WHICH, IN TURN, ALLOWS QI TO CONDUCT. AS THE COLLECTOR OF QI APPROACHES OV, CR2 CONDUCTS CHARGING C3, AND MAINTAINING Q2 IN CUT-OFF. Q2 REMAINS CUT-OFF UNTIL C3 CAN DISCHARGE SUFFICIENTLY THROUGH R3 TO PERMIT CONDUCTION OF Q2. THE PERIOD OF CONDUCTION OF QI IS PRIMARILY DETERMINED BY THE SIZE OF C3 AND R3.



CARD CONNECTIONS ARE REPRESENTED BY LETTERS TEST POINTS ARE REPRESENTED BY NUMBERS

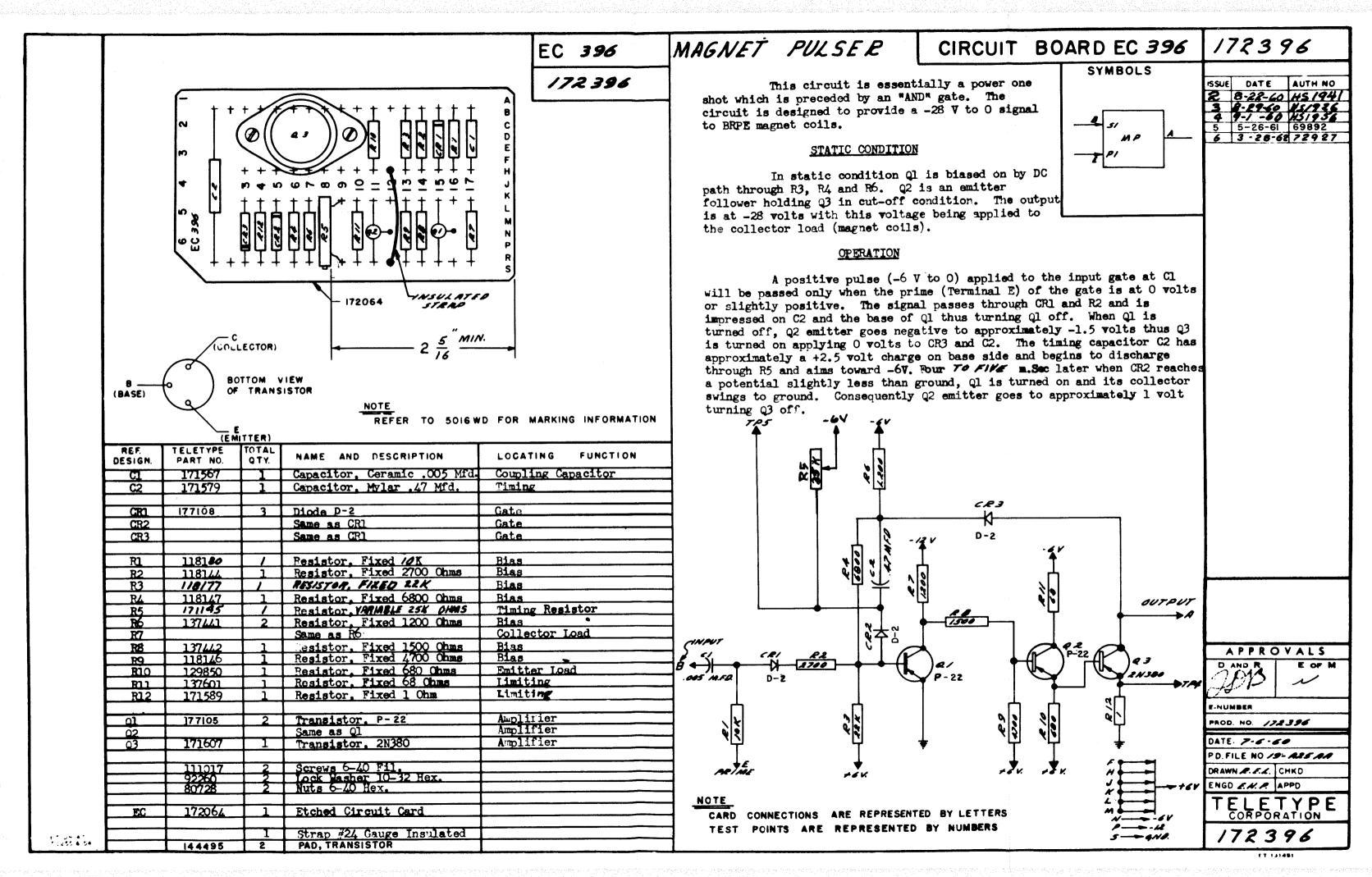
D AND E-NUMBER PROD. NO. 172395 DATE: 3-1-60 P.D. FILE NO. 1-11.134AA

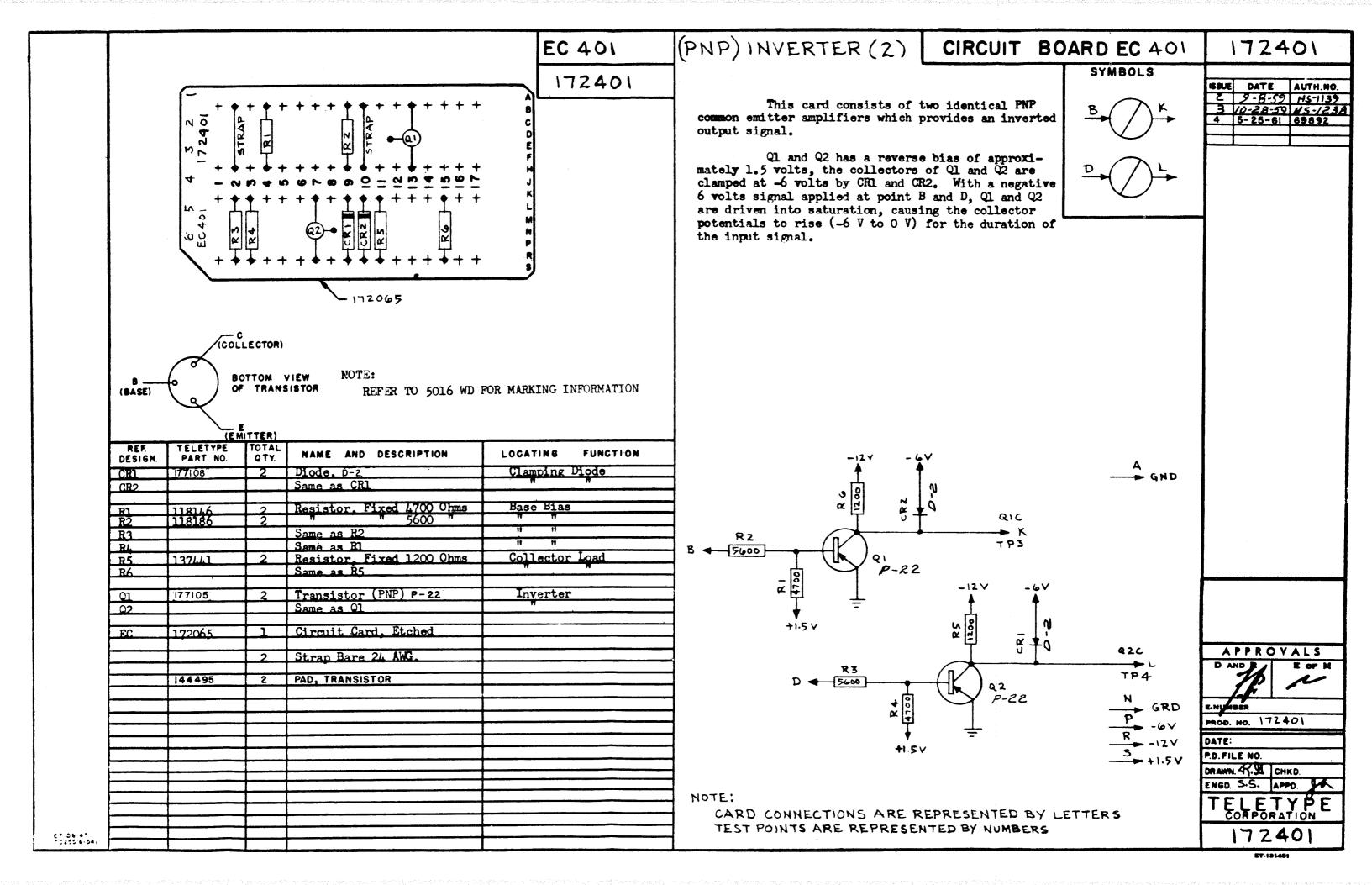
CHKE DRAWN, AB ENGD E.H.P APPD.

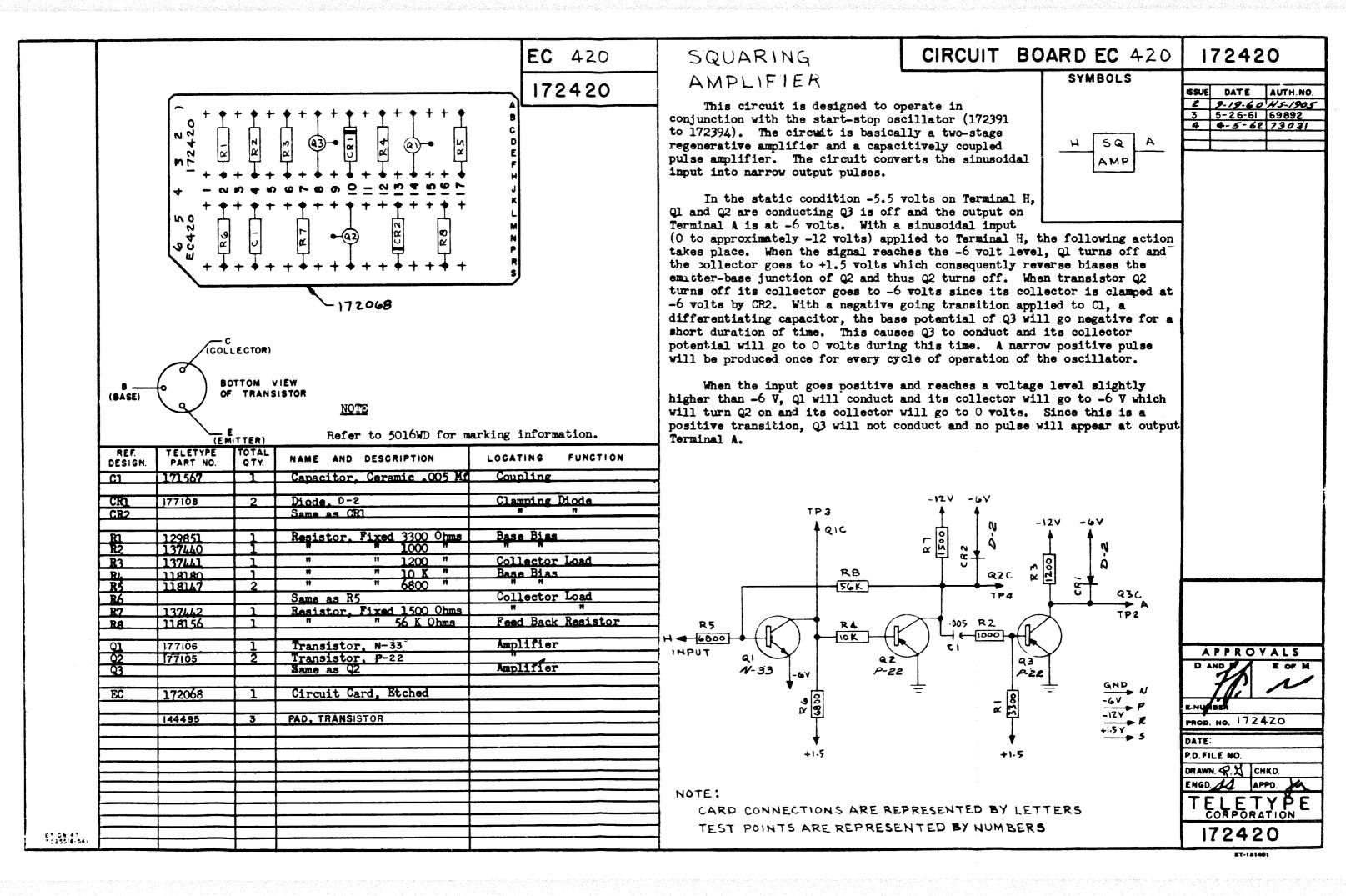
APPROVALS

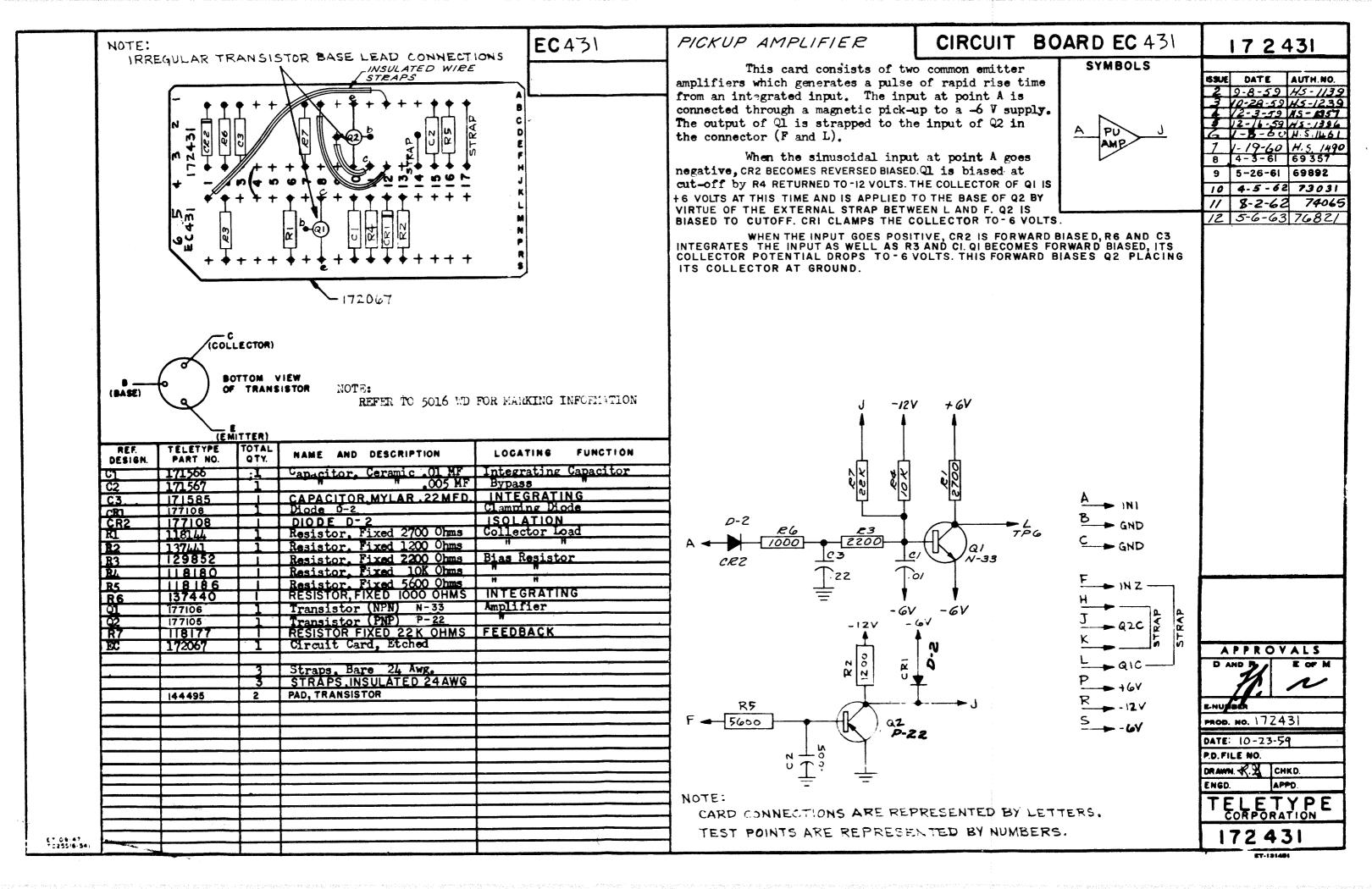
E OF M

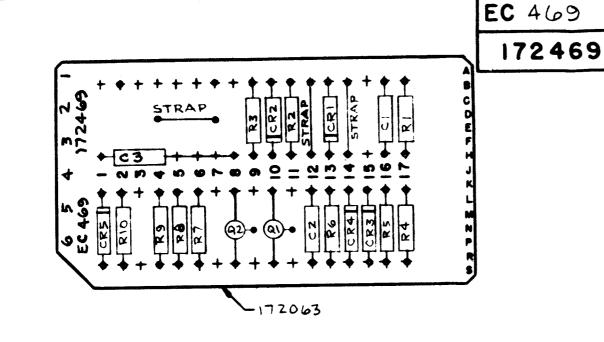
CORPORATION 72395











NOTE:

REFER TO 5016 WD FOR MARKING INFORMATION

OF TRANSISTOR

BOTTOM VIEW

(COLLECTOR)

(BASE)

ET 09:47 *C255(6-54)

TELETYPE PART NO. TOTAL NAME AND DESCRIPTION LOCATING FUNCTION QTY. DESIGN. Capacitor, Ceramic .002 MF Coupling 177332 Feed Back .001 /7733/ Q2 MF Timing TUBULAR C3 137311 Coupling CRO CRO CRO 177108 Diode, D-2 DIODE D-2 Gate Same as CR2 Clamp CR4. Same as CR2 Gate Same as CR2 Resistor, Fixed 22K Ohm Gate B1 R2 118177 " 1500 " Bias 137442 11 8200 H Timing 13744 1 R3 " 1200 Ohm Collector Load R₂ 137441 Same as RL Resistor, Fixed 3300 0hm Feed Back 129851 Bias 2700 H עופוו 118180 Common Emitter Load 51 Ohm. R9 143656 Bias 6800 Ohm RIO 1118147 Transistor P-22 Switch 177105 Same as Q1 Circuit Card Etched STRAP 24AWG BARE 172063 PAD, TRANSISTOR 144495

CIRCUIT BOARD EC469

FIXED ONE-SHOT

100 MS

The purpose of this circuit is to generate a pulse of 100 micro seconds in width in response to an input. Normal (positive going) and inverted outputs are provided.

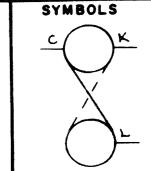
The quiescent state of this circuit is that Q2 is saturated, receiving its bias current primarily through R2 and R10 connected in parallel with CR5 and Q V and the collector of Q1 is -0 V. Q1 is maintained cut-off by cross coupling of R6 and R7 returned to +1.5V, holding the base potential of Q1

at approximately +1 V. The common emitter potential is 0 V since Q2 is saturated.

Capacitor C1, R1 and CR1 combine to form an inhibit gate, whereby when -6 V is applied at point J, inputs received at point C will fail to trigger the circuit. Conversely the circuit is enabled when point J is

returned to 0 V since CRl will now pass positive going transitions.

The circuit is triggered as follows: A positive transition applied at point C drives Q2 into cut-off which, in turn, allows Q1 to conduct. As the collector of Q1 approaches O V, CR2 conducts charging C3, and maintaining Q2 in cut-off. Q2 remains cut-off until C3 can discharge sufficiently through R3 to permit conduction of Q2. The period of conduction of Q1 is primarily determined by the size of C3 and R3.



BUE DATE AUTH.NO.

2 6-30-56 HS-1040

3 9-8-59 MS-1/39

4 1/0-24-59 MS-1/234

5 1/-1/-59 MS-1/234

7 5-26-61 69892

8 1/-16-6/ 7/626

172469

-124 INVERTED 1-6V NORMAL TURTUO OUTPUT TP21K TP / LI œ 920 CR3 4 CRZ 0 TO 9 .002 91 Q2 P-ZZ 8 0 X 22 ALL DIODES 0-2 +1.54 NOTE:

CARD CONNECTIONS ARE REPRESENTED BY LETTERS TEST POINTS ARE REPRESENTED BY NUMBERS

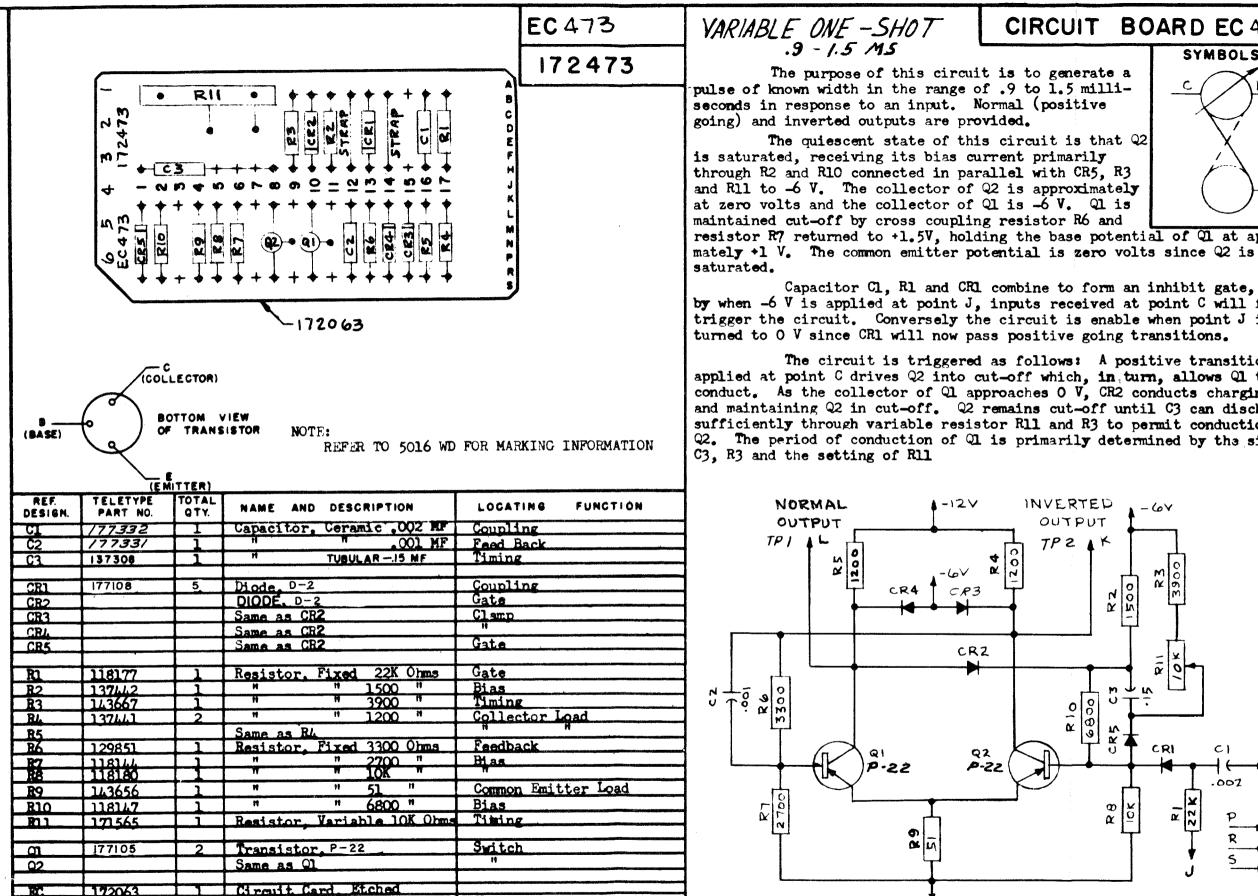
APPROVALS
DAND E OF M
ENUER
PROB. NO. 172469

DATE: P.D. FILE NO.

DRAWN. Q. S. CHKO. 7.15 ENGD. J. D. APPO.

TELETYP CORPORATION 172469

ET-121481



SCREW. 437-2X56 FIL

NUT 2 X 56 HEX.

PAD, TRANSISTOR

STRAP 24AWG BARE

1178

ET-06-47 TC255(6-54)

110446

144495

VARIABLE ONE -SHOT .9 - 1.5 MS

CIRCUIT BOARD EC 473

172473

The purpose of this circuit is to generate a pulse of known width in the range of .9 to 1.5 milliseconds in response to an input. Normal (positive going) and inverted outputs are provided.

The quiescent state of this circuit is that Q2 is saturated, receiving its bias current primarily through R2 and R10 connected in parallel with CR5, R3 and R11 to -6 V. The collector of Q2 is approximately at zero volts and the collector of Ql is -6 V. Ql is maintained cut-off by cross coupling resistor R6 and resistor R7 returned to +1.5V, holding the base potential of Q1 at approxi-

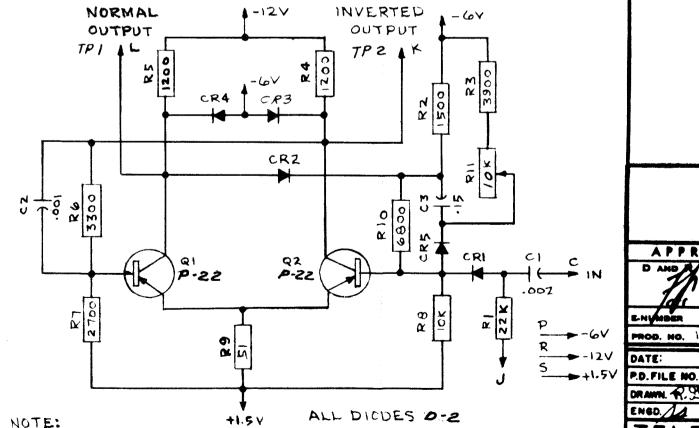
SYMBOLS

2 6-30-59 HS-1040 3 9-8-50 H5-1139 4 10-28-59 H5-1238 5 11-17-39 175-1238 6 11-25-89 115-13/ 5-26-61 69892 11-16-61 71626 4-5-62 73031 10 3-2-63 76172 3-20-63 76349

SSUE DATE AUTH NO.

Capacitor Cl. Rl and CRl combine to form an inhibit gate, whereby when -6 V is applied at point J, inputs received at point C will fail to trigger the circuit. Conversely the circuit is enable when point J is returned to 0 V since CR1 will now pass positive going transitions.

The circuit is triggered as follows: A positive transition applied at point C drives Q2 into cut-off which, in turn, allows Q1 to conduct. As the collector of Q1 approaches O V, CR2 conducts charging C3, and maintaining Q2 in cut-off. Q2 remains cut-off until C3 can discharge sufficiently through variable resistor R11 and R3 to permit conduction of Q2. The period of conduction of Q1 is primarily determined by the size of C3. R3 and the setting of R11

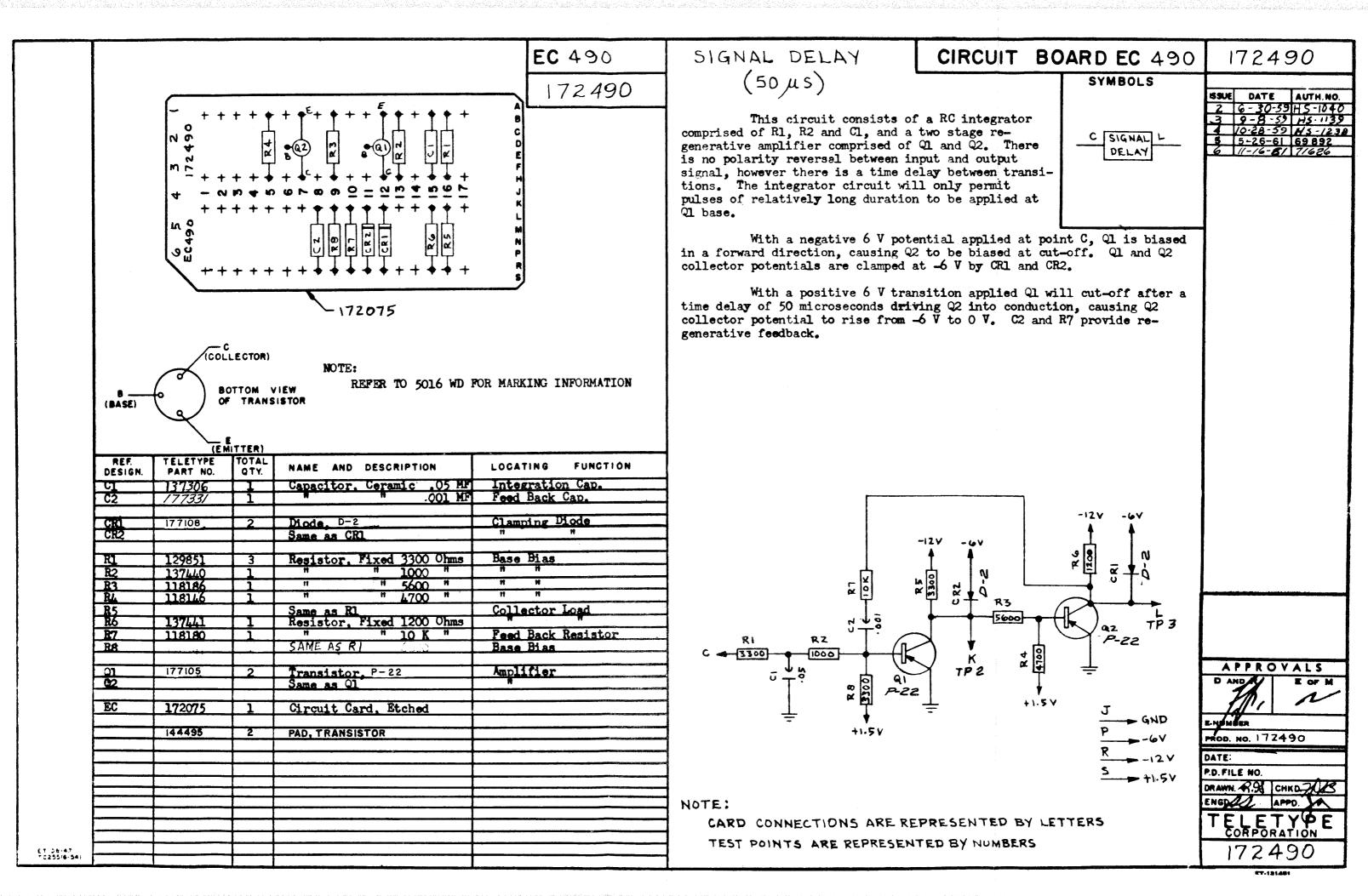


DRAWN. R.S. CHKD.

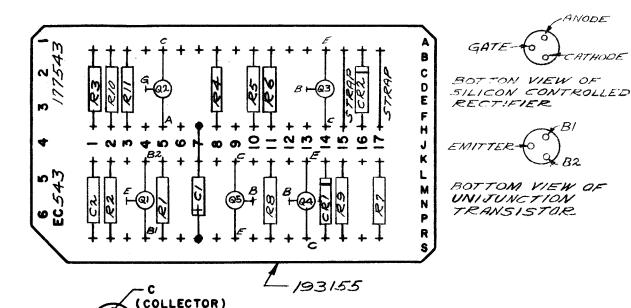
APPROVALS

PROD. NO. 172473

CARD CONNECTIONS ARE REPRESENTED BY LETTERS TEST POINTS ARE REPRESENTED BY NUMBERS







NOTE:

INFORMATION

REFER TO 5016WD FOR MARKING

BOTTOM VIEW

(EMITTER)

OF TRANSISTOR

(BASE)

ET109147 TC255(6-54)

REF. DESIGN	TELETYPE PART NO.	TOTAL QTY.	NAME AND DESCRIPTION	LOCATING FUNCTION
Rl	118162	1	Resistor fixed 270K ohms	Timing
R2	137603	1	" 510 ohms	Base 1 Load
R3	137441		" 1.2 K ohms	Bias
R4	143659	2	" " 560 ohms	Divider
R5	118724	1	" " 220 ohms	Divider
R6	129852	1	" 2.2 K ohms	Current Limiter
R7	137443	1	n n 1 ₉ 8 K ohms	Base Bias
RR			Same as R4	Collector Load
R9	118186		" " 5.6 Kohms	Bias
R10	137438	1	" " 100 ohms	Current Limiter
Rll	118169	1	" 1 meg.	Switch by pass
Cl	148165		Capacitor 22 MF ± 20 %	Timing
C3	177107	1	" _l MF	Coupling
CRI	177108	2	Diode D2	Input Diode
CR2			Same as CRL	
Ol	177610	1,	Unijunction	Oscillator
02	177100	1	Silicon Controlled Rec. SPl	Switch
Q 3	177224	2	Transistor 2N398A	Power
O/r	177105	1	Transistor P22	Amplifier
Q.5			Same as Q3	Power
Strap		2	Strap-Bare #24 AWG	
	144495	5	Pad, Transistor	
BC			Circuit Card - Etched	
EA/	193155	11	OTLOUTE CALG - Proued	<u> </u>

CIRCUIT BOARD EC

SYMBOLS

177543

TIME DELAY RELAY DRIVER

This circuit consists basically of two relay drivers, one of which is operated by a time delay circuit.

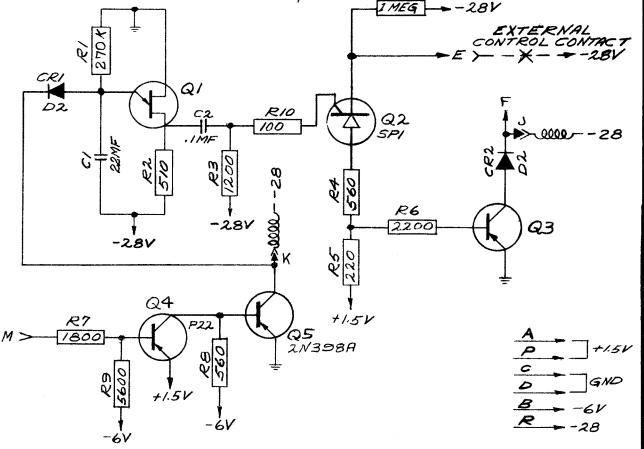
In the static or "off" condition, M is at 0 volts or more negative and Q4 is conducting holding Q5 off.

Transistor Q5 collector output (K) is connected to a relay biased to -28 volts. Diode CR1 is forward biased and a small amount of current flows from ground via R1, CR1 and relay to -28 volts. Unijunction Q1 and SCR Q2 are off holding Q3 off. Collector load of Q3 is a relay biased to -28 volts.

D.R.D. K

When a +5 volt signal or greater is applied to input M, Q4 is turned off, Q5 is saturated and output K goes to ground energizing the relay (collector load) and reverse biasing CR1. Capacitor Cl begins to charge toward ground via R1. At some voltage (less than half the voltage across Q1) the unijunction will be triggered discharging Cl via emitter and R2. A positive pulse is applied to C2, SCR (Q2), and the SCR will turn on if the external control contact is closed applying a negative voltage on the base of Q3 switching Q3 on which places O volts at output J and the second relay is energized. Q3 will be turned off when SCR is cut off by the opening of external control contact. Q5 is turned off by placing a O volt signal or more negative on M input. Output F of Q3 provides lead which permits by-passing the circuit card in its intended application.

The delay of this timer may vary between 4.5 to 8.5 seconds depending upon capacitor tolerances and operating temperature. 2//



NOTE:

CARD CONNECTIONS ARE REPRESENTED BY LETTERS
TEST POINTS ARE REPRESENTED BY NUMBERS

DATE: 8-24-62 P.D. FILE NO. 1-11.13499 DRAWN 59 CHKB (1)

D AND B

NUMBER

ENGD. EHP APP

TELETYPI CORPORATION 177543

APPROVALS

PROD. NO. 177543

E OF M